A design strategy for analyzing signal integrity in DDR3 bus of high speed embedded systems

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ABSTRACT

A complex modern embedded system using a multi-core Central Processing Unit (CPU) toward a compact integrated design in a single Printed Circuit Board (PCB). One of the biggest challenges of the design is to meet the Signal Integrity for high speed Double Data Rate 3 Synchronous Dynamic Random-Access Memory (DDR3) bus. A typical strategy to solve the challenge is the simulation on the computer, but this is not always an effective solution as has a gap between simulation software and practical PCB. The gap is correlated to localized changes in copper density within the PCB and characterization of heterogeneous materials in PCB that could lead to differences in the real PCB. The purpose of the research presents an analysis methodology to design DDR) memory interfaces in high speed embedded systems, related to Signal Integrity and the impact of copper density on PCB trace impedances to overcome these challenges. Moreover, the presented design methodology is also applied to the next generation DDR as well as other styles of CPU.

Keywords: Signal Integrity; PCB; DDR3; Trace Impedance.

1. INTRODUCTION

Various issues of Signal Integrity (SI), Power Integrity (PI), and Electro-Magnetic Interference (EMI) as well as routing complexities and component density are challenges in the high quality embedded design process. To produce high quality PCB, hardware design and development process of the embedded system are classified into five steps: schematic design, board and layout design, SI and PI Simulation, fabrication, testing.

Schematic and PCB layout design is the process from a dedicated concept phase before builds to the product development phase composed of builds. PCB manufacture and fabrication is the important step to ensure the design quality. The quality of the PCB is affected by the technologies of the provider, such as PCB drilling, etching quality and manufacture variation. The SI and PI simulation processes will debug errors and verify the improvement solution after the test of each build.

Issues in PCB layout step begin with the component placement and routing traces. PI and SI simulation results constraints determine the placement of components on the PCB. Thermal and mechanical problems have not yet been mentioned in this research. DDR3 bus design in the embedded system often encounters a variety of signal integrity problems. This design has to consider routing trace, termination and layout design, stability of the power supply. Challenges of SI in PCB design include issues as SI for single end or differential pairs; crosstalk, power and distribution nets and EMI. One of the most important issues facing the PCB design is the SI, which may relate to reduce other effects on the PCB board. PI challenges can be reduced by good power supply design.

However, the reflection problems in signal integrity of digital high speed circuits are one of the most important challenges. Reflection in the PCB design is the result of mismatch of the impedance. In the T-topology [1], the impedance of the branch is double the root in order to match

the impedance, but the width of the trace in DDR with the popular ball grid array package is thinner than 10 mil. Hence, it is difficult to be more than twice or four times of 10 mil in the modern PCB. This problem is overcome by applying Fly-by topology for third generation DDR and next generations. In the Fly-by topology, the command and address signals are routed in series with each of the memory modules along with appropriate termination at the end.

In the research [2, 3], SI simulation using statistic analysis is applied to reduce the development period for manufacturing low cost and small size PCB. The recent paper [4] demonstrated many challenges in SI and PI simulations in the high speed embedded system design and proposed a practical solution to solve issues. Traditional SI and PI co-simulation was researched by papers [5, 6] to provide a more accurate solution. In the research [7], SI and PI co-simulation was applied to optimize Power Distribution Network (PDN) for achieving high performance in the high speed digital circuit design.

However, an issue critical to the high speed DDR busses is that the practical bus impedance is shifted to the simulation on the computer and result is the parameters of PCB being out of design. Recently, some research has shown that shifts in measured impedances across a PCB layer are correlated to the copper density in the PCB panel. Hence, additional research about the copper density across the fabrication panel to minimize impedance shifts between simulation and practical product is necessary.

Consequently, a case study for high speed buses under the platform of a DDR3 memory module in the embedded system using Field Programmable Gate Array (FPGA) ZYNQ-7020 demonstrates the proposed SI/PI co-simulation strategy. Our design strategy incorporates SI and PI co-simulation with considering the copper density in the PCB panel to show the strategy that addresses the challenges of high speed design for embedded systems. This paper is organized into four parts. The next part shows the background of the simulation in the PCB design, while part III will focus on the SI simulation as well as analysis of the SI issues of the DDR3 memory. Finally, a conclusion and future works are given in part IV.

2. SYSTEM OVERVIEW

The demand for miniaturization of embedded system is increasing in military applications especially precision guided weapons and small drones. In recent years, System in Package using Zynq® 7000 and DDR3 memory has the advantages of small size and ultra-low power consumption compared with the other embedded systems using ARM cores.

FPGA ZYNQ-7020 was interfaced with two 512 MB DDR3 SDRAM through 32 bit wide data bus. From the datasheet of DDR3, the command, address and control signals operate at several times lower data speed than the clock signal. Hence, the paper only focuses on the analysis of the clock signal and other signal have not been mentioned in this paper.

The current state of embedded hardware design is unseparated from the layout and assembly process for the small volume of mass products. In the modern complex embedded system design, the tight coupling between computational performance, high speed and low power requires smaller ball-grid array packages with increased adoption of radiation-tolerant devices that understands all aspects associated with design decisions.

In order to obtain the accuracy impedance of the PCB trace, a complex two-dimensional electromagnetic field solver is calculated, but this is mainly convenient for theoretical analysis. In the actual design, impedance of the PCB trace can be calculated by the below well-known equivalent formula [8]:

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{0.8W + T}\right] \tag{1}$$

Where ε_r is the dielectric constant of the PCB material. H, W and T is the height, width and thickness of the PCB trace, respectively.

To reduce the difference between simulation and real parameters in PCB design, it is available to consider the copper density and copper density transitions drive for PCB design. In the practical, the research [9] trace impedance of four layers PCB is affected by the copper density. When a digital circuit's speed becomes faster, the impedance mismatch phenomenon will be increased and lead to the real impedance shifts away from the optimal impedance. However, the copper density of PCB traces is not easy to describe by theoretical functions. Minimizing impedance offsets can be implemented by the experiences of good design engineers.

SI analysis was considered at each stage of the design. From the recommendation of the producer, optimal parameters of lengths of data bus lines, the maximum length of parallel bus, via dimensions, etc., were determined during layout design. If the given routing strategy results can not meet a demand, the layout simulation is repeated and the process is performed again until meeting the constraints of the layout design. When the routing design is completed, the layout SI simulation is executed through Eye Diagram and timing demands are verified. If the layout design meets all the technical specifications, the board design is achieved. If the design is not, the mention process is executed again.

3. SIMULATION RESULTS

A key part of memory system design is detailed design simulation. Experience has shown that small variations in the resistance value of the resistor can have a significant impact on the reliability of the memory system itself. The simulation of the design of the memory system should include the load effects in cases when any instrument is connected to the system prototype. Also, the simulation should analyze the signals in the test points when connecting the instrument. The correct data window displays and changes its values along the signal flow, from the memory controller to the DDR3 pins.

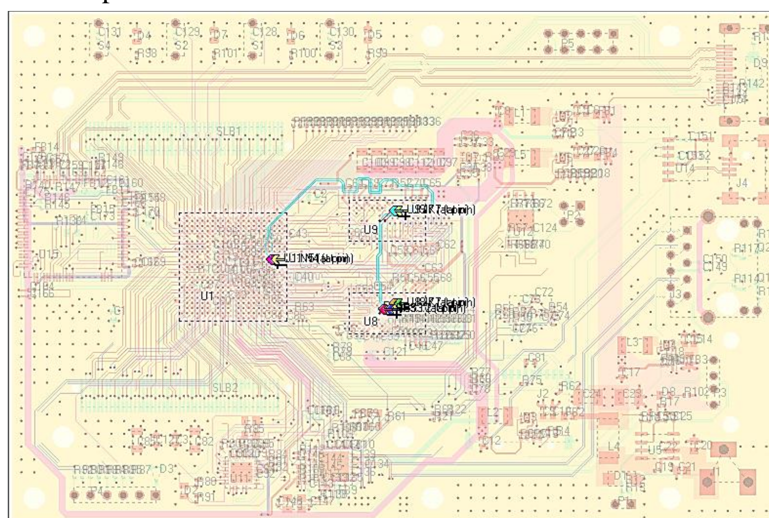

Figure 1. *Timing signal on embedded system board using FPGA ZYNQ-7020 and DDR3.*

Each manufacturer provides a signal shape specification in its documentation that guarantees that the memory chip will work correctly. The signal, in addition to the frequency, must meet several other parameters, such as the amplitudes of the direct current and sinusoidal components of the voltage. In order for the designer of the printed circuit board to make sure that the shape of the signal is correct, it is necessary to perform a series of simulations in order to check whether each signal meets the requirements.

Figure 2 shows a part of the simulation program HyperLynx, where it can be seen that the line over which the simulation will be performed is selected. The differential line in simulation is DDR-CLK_P/N. The timing signal expression changes gradually over time. The distortion of the signal is caused by the mismatching impedance of the transmission line.

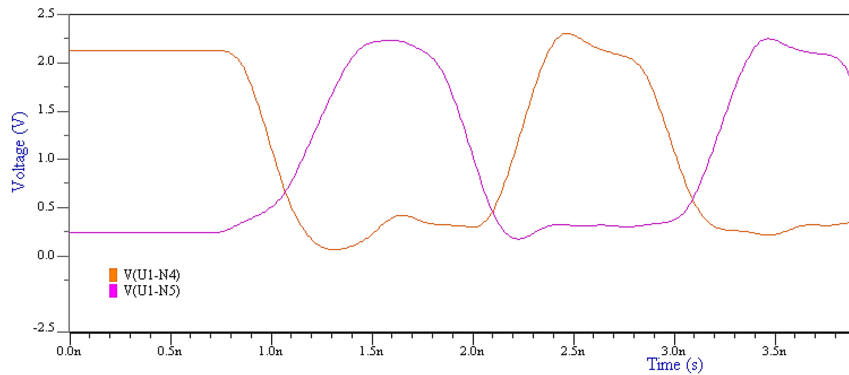

Figure 2. *Scope of the timing signal.*

The timing channel of clock signal was stimulated for eye diagram simulation at 1066 Mbps speed. Eye diagram of clock signal has been illustrated in this section using a 1.5 Volts, 533 MHz as shown in the following figure.

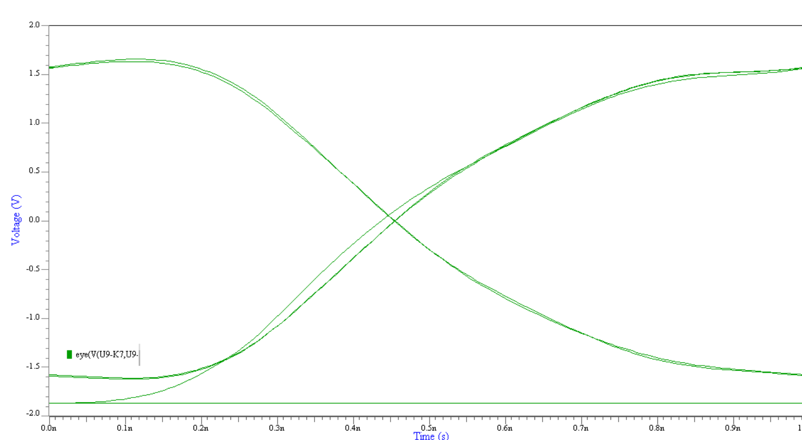

Figure 3. *Eye diagram of the timing signal.*

The eye diagram shows an eye height of 1361 mV. As a result, this is smaller than the recommendations in the manual document of the producer. The jitter of the timing signal is less than one and a half times as DDR3 specification documents is provided in JESD79-3F standard [10]. Timing clock propagating along the transmission line on the PCB board experiences significant high frequency loss from capacitive reflections at DRAM input nodes as it passes through each node. It is seen in the figure that eye opening at the node toward back of the transmission line is described more from a high frequency loss as seen in slower transition edges. Eye diagram of the simulation illustrates eye opening data are specific to a PCB routing for timing channel configuration used in this test.

One of the main characteristic parameters of the transmission line is the trace impedance. The characteristic impedance not only affects crosstalk and reflection but also impacts the SI of the design. In the simulation, the characteristic impedance of the timing transmission line represents scope in the time. Through the following figure, the characteristic impedance in the time can be extracted or derived.

The trace impedance of the main controller as Tx side is 46.914 Ohm, which is met all the technical specification. The trace impedance of the DDR3 as Rx side is 45.161 Ohm. Figure 4 and figure 5 illustrate the differential impedance of the Tx side and Rx side is small. Hence, impedance matching of the PCB trace connecting FPGA and DDR3 memory modules is archived to prevent reflections that can cause glitches on the timing channel.

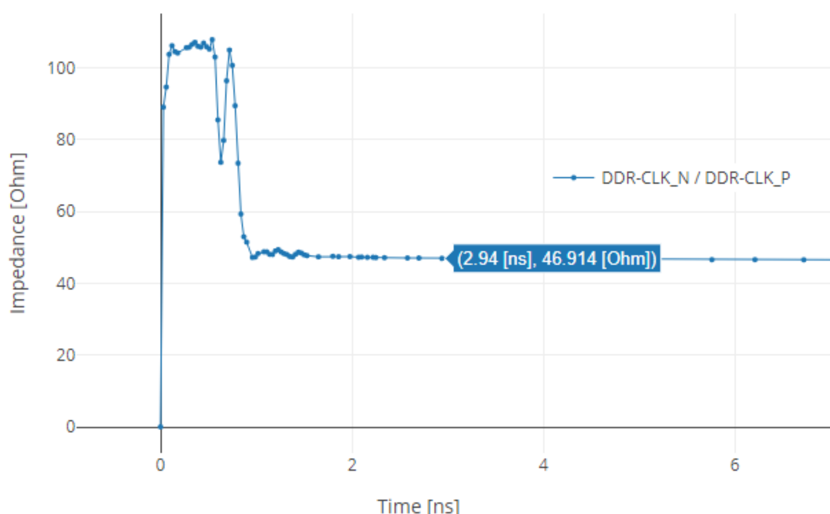

Figure 4. *The TX side impedance of PCB trace in the time.*

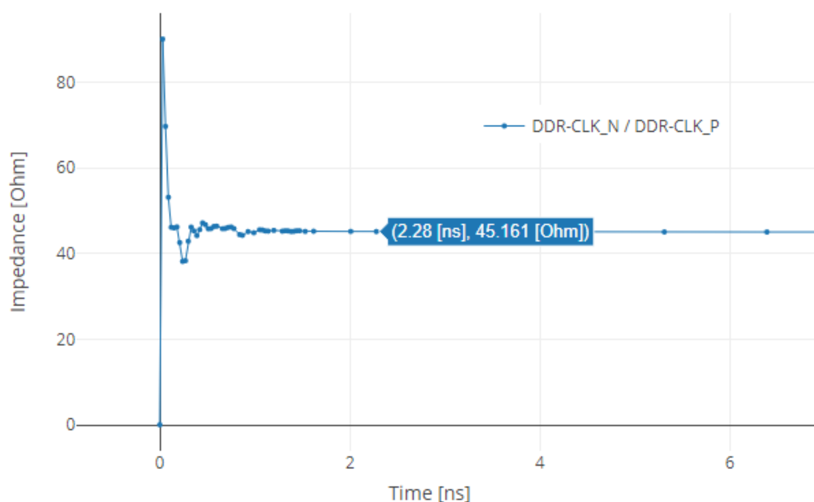

Figure 5. *The Rx side impedance of PCB trace in the time.*

The attenuation of the clock signal is analyzed to extract the network parameter of power and signals over a wide range of frequencies. The simulation in the software HyperLynx will give accurate results over a wide range of frequencies (25 MHz to 10 GHz) with less simulation time than the other simulation software. Figure 5 demonstrates the attenuation coefficient of timing signal over the frequency range. The length of the transmission line of timing signal is 2.87 inches. As shown in

the following figure, an acceptable attenuation of about 4.5 dB is inserted in the transmission line for the frequency under 1.5 GHz. It means that the DDR4 is also used for this result.

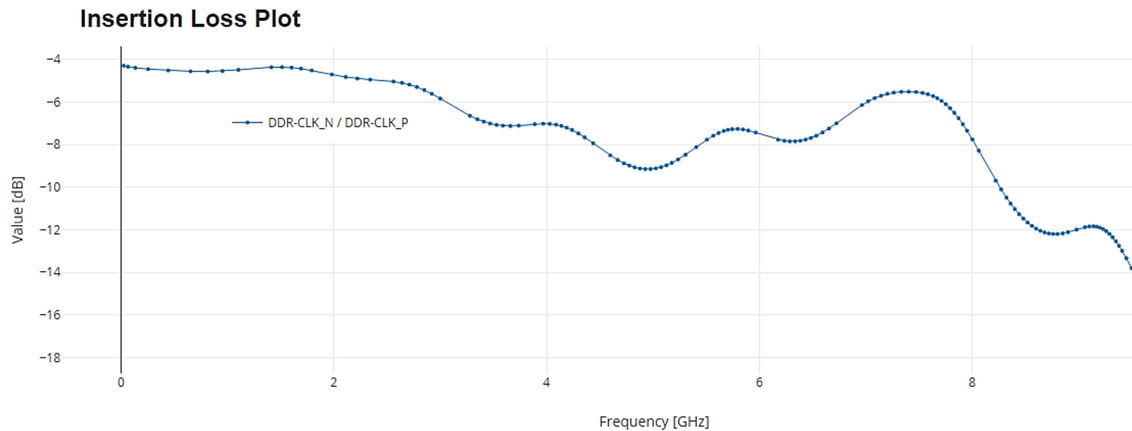

Figure 6. *Attenuation of the clock signal in the frequency domain.*

4. CONCLUSIONS

In this paper, the entire process of designing the memory interface in modern embedded systems is explained in detail. An overview of the realized steps is given. Then, the process of designing and simulating the PCB of ZYNQ-7020 and DDR3 is presented. To improve signal integrity, DDR3 SDRAM memory modules adopt Fly-by topology for commands, addresses, control signals, and clock signals. The improvement in our strategy identifies the additional step to consider the effect of copper density and copper density transitions drive in the PCB design process. The process of simulating the design is specially addressed which is tested before manufacturing the product. Finally, the results of the simulations confirmed the success of the design and strategy for guaranteeing product reliability. Moreover, the methodology and simulation used in the article also may be applied to the higher generation of DDR3.

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TÓM TẮT

Chiến lược thiết kế phân tích tính toàn vẹn tín hiệu trong bus DDR3 trong các hệ thống nhúng tốc độ cao

Hệ thống nhúng hiện đại phức tạp sử dụng bộ xử lý (CPU) đa lõi hướng tới thiết kế tích hợp nhỏ gọn trong một bảng mạch in (PCB) duy nhất. Một trong những thách thức lớn nhất của thiết kế là đáp ứng Tính toàn vẹn tín hiệu cho bus bộ nhớ truy cập ngẫu nhiên thế hệ 3 (DDR3) tốc độ cao. Chiến lược điển hình để giải quyết thách thức này là mô phỏng trên máy tính nhưng đây không phải lúc nào cũng là giải pháp hiệu quả vì có một khoảng cách giữa phần mềm mô phỏng và PCB thực tế. Khoảng cách này có liên quan đến những thay đổi cục bộ về mật độ đồng trong PCB và đặc tính của các vật liệu không đồng nhất trong PCB có thể dẫn đến sự khác biệt về trở kháng trên PCB thực. Mục đích của nghiên cứu là trình bày phương pháp phân tích để thiết kế giao diện bộ nhớ DDR3 trong các hệ thống nhúng tốc độ cao, liên quan đến Tính toàn vẹn tín hiệu và tác động của mật độ đồng đến trở kháng đường mạch PCB để vượt qua những thách thức này. Hơn nữa, phương pháp thiết kế được trình bày cũng được áp dụng cho DDR thế hệ tiếp theo cũng như các kiểu CPU khác.

Từ khoá: Toàn vẹn tín hiệu; PCB; DDR3; Trở kháng đường mạch.