
Research on technical solutions for digital signal processing to enhance the reception quality of air defense radar systems

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ABSTRACT

The paper presents the signal processing algorithm, hardware design solution, and software development of the digital signal processing module for linear frequency modulated signals to improve the signal-to-noise ratio and reduce computational overload in the system. The proposed signal processing algorithm performs direct analog-to-digital conversion of two quadrature channels, downsampling filtering, optimization filtering, and signal correlation compression filtering. The selected functional components feature several advantages such as high gain, high speed, and ready availability in the market. The hardware design and software development were carried out following a survey–simulation–prototype process, ensuring high logical coherence and systematic integration. The final product has been successfully validated on both test benches and radar systems.

Keywords: Digital signal processing; Linear frequency modulation; CIC filter; FIR filter.

1. INTRODUCTION

The rapid advancement of digital technology has enabled the design of digital receivers for modern transmitter systems, offering many outstanding advantages over analog receivers. These advantages include the flexibility to reconfigure operating parameters and connect with peripheral devices, the ability to flexibly choose intelligent processing algorithms thanks to software programmability, increased cost-effectiveness, reduced device size and weight, lower power consumption, and improved ease in controlling system faults [6]. In addition, digital technology enables modern transmitter systems to extend their operating frequency range and flexibly use wideband or ultra-wideband transmission signals in combination with modern signal processing techniques. In Vietnam, the research, design, and manufacturing of modern transmitter systems have developed rapidly and achieved significant accomplishments in recent years. Notably, this progress is exemplified by the successful design and production of the VRS-2DM 2D air defense radar and the tactical 3D air defense system by the Military Telecommunications Industry Corporation VIETTEL.

Following this approach, the paper presents the solution (including hardware design, software development, and the basis for selecting the signal processing algorithm) in the design and manufacture of a digital signal processing module for linear frequency modulated signals at an intermediate frequency, aimed at increasing the signal-to-noise ratio and reducing the system's digital computational overload. The subject of the study is the radar digital signal processing module. The module's input signal model is a linear frequency modulated signal. The research outcomes of the paper provide a scientific foundation for widespread application in the design and manufacture of digital receivers for many modern transmitter systems. The remainder of the paper is organized as follows: Section 2 analyzes the solution in designing and manufacturing the module; Section 3 presents the experimental results; Section 4 concludes the paper.

2. SOLUTION IN THE DESIGN AND MANUFACTURE OF THE MODULE

2.1. Hardware design and software development

2.1.1. Hardware design

The hardware of the digital signal processing module is categorized by function and task to reduce design complexity and simplify system error control. The circuit components include: power generation and distribution circuits, control and fault diagnosis circuits, connection and data transmission circuits, synchronous signal generation circuits, and signal processing circuits [2, 3, 5]. Among them:

- The power generation and distribution circuit type PTH08T240WAD creates filtered and stabilized power supplies.
- The control and fault diagnosis circuit of the Stratix III DSP type ensures proper control and error monitoring of the module's functional components. The monitored statuses include assessing component failures, overcurrent conditions, or power supply voltage deviations.
- The synchronous signal generation circuit employs a crystal oscillator with high frequency stability.
- The digital signal processing circuit comprises an ADC driver (differential amplifier) of the THS770012 type with a gain ranging from 10 to 14 dB, along with 16-bit A/D converter based on ADS5483.
- The foundation of the FPGA firmware is built on the NIOS II soft-core processor, with communication interfaces connected according to the Ethernet standard (TSE MAC, SGDMA Rx/Tx core, packet assembler), as well as GPIO and timer modules.

The hardware of the digital signal processing module has been designed and manufactured as a very complex board featuring a total of 14 gold-plated layers, with board dimensions of 220x230 mm. It meets very strict requirements for impedance matching and routing according to high-speed PCB design and fabrication processes, and it was produced and assembled at the FAB-9 Vietnam factory (figure 1).



Figure 1. Digital signal processing module for the transmitter.

2.1.2. Software development

All of the design software and micro-programs are implemented using Quartus II version 10.1 and its IP COREs. The software architecture handles control, distribution of address and data streams, and specifies the operating frequency range of the embedded processing core in NIOS II SOPC BUILDER. The control software's source code is written in Quartus II using the VHDL hardware description language and incorporates IP COREs. Functions include:

- Access flash memory, configure the Ethernet physical layer, and set the status of GbE switches.
- Receive synchronization information and distribute it to the FPGA board.

- Micro-programs for the signal processing circuit perform tasks including digitizing the intermediate frequency signal, converting the multi-channel transmission signal to baseband, filtering and compressing the signal, and packaging the data.

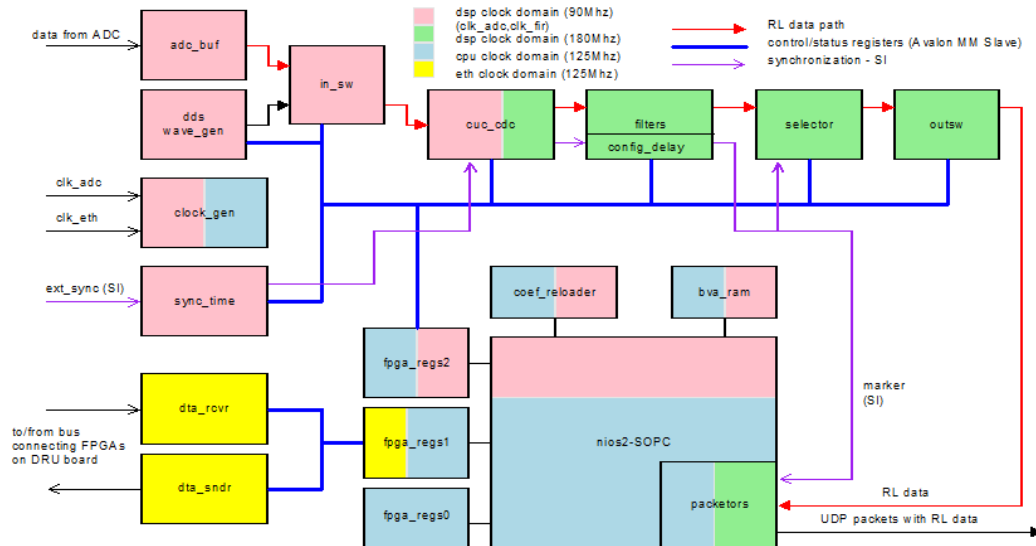


Figure 2. Software architecture diagram of the module.

In figure 2, the diagram illustrates the software architecture of the module. The pink area represents the operating domain of the processing channels, which run at a specified speed of 90 MHz. The green blocks indicate the operating domain of the digitization processors, operating at 180 MHz, while the remaining blocks function in the 125 MHz frequency domain.

2.2. Selection of the digital signal processing algorithm

The input signal model is a linear frequency modulated pulse signal described as follows:

$$s(t) = S_0(t) \cos[2\pi(f_0 - \Delta f / 2)t + bt^2]$$

where, f_0 is the center frequency, Δf is the frequency deviation within the pulse, b is the frequency slope, and $S_0(t)$ is the envelope function of the signal ($S_0(t) = 1$ where $0 \leq t \leq T$; $S_0(t) = 0$ otherwise). The frequency deviation is defined as the product of b and the signal duration T . The structural diagram of the digital signal processing algorithm is shown in figure 3. The tasks of the digital signal processing algorithm include:

- Analog-to-digital conversion of the signal;
- Conversion of the signal to baseband and execution of digital phase demodulation;
- Signal decimation and digital filtering;
- Signal compression in time domain;
- Clutter filtering using MTI algorithm;
- Target radial velocity filtering using MTD algorithm;
- Monitoring of the frequency-dependent active interference;
- Automatic detection and measurement of target coordinate parameters [4, 7].

To obtain the quadrature components of the signals, the original signal is multiplied with sine and cosine signals of the same frequency. This method requires only one ADC converter instead of two. In each quadrature channel, the signal is downconverted to baseband using a mixer. A CIC filter then performs sample decimation. The output from the CIC filter is fed to a

compression filter that compresses the pulse signal in time by cross-correlating the transmitted signal (in baseband) with the reflected signal. The result after the compression filter is passed to a Fast Fourier Transform (FFT) module, where further processing evaluates the target's radial velocity and filters out clutter (i.e., digital filtering of moving targets against the background clutter). Finally, the signal is sent to an automatic target detection and coordinate measurement unit, and the target information is forwarded to the transmitter's information processing system.

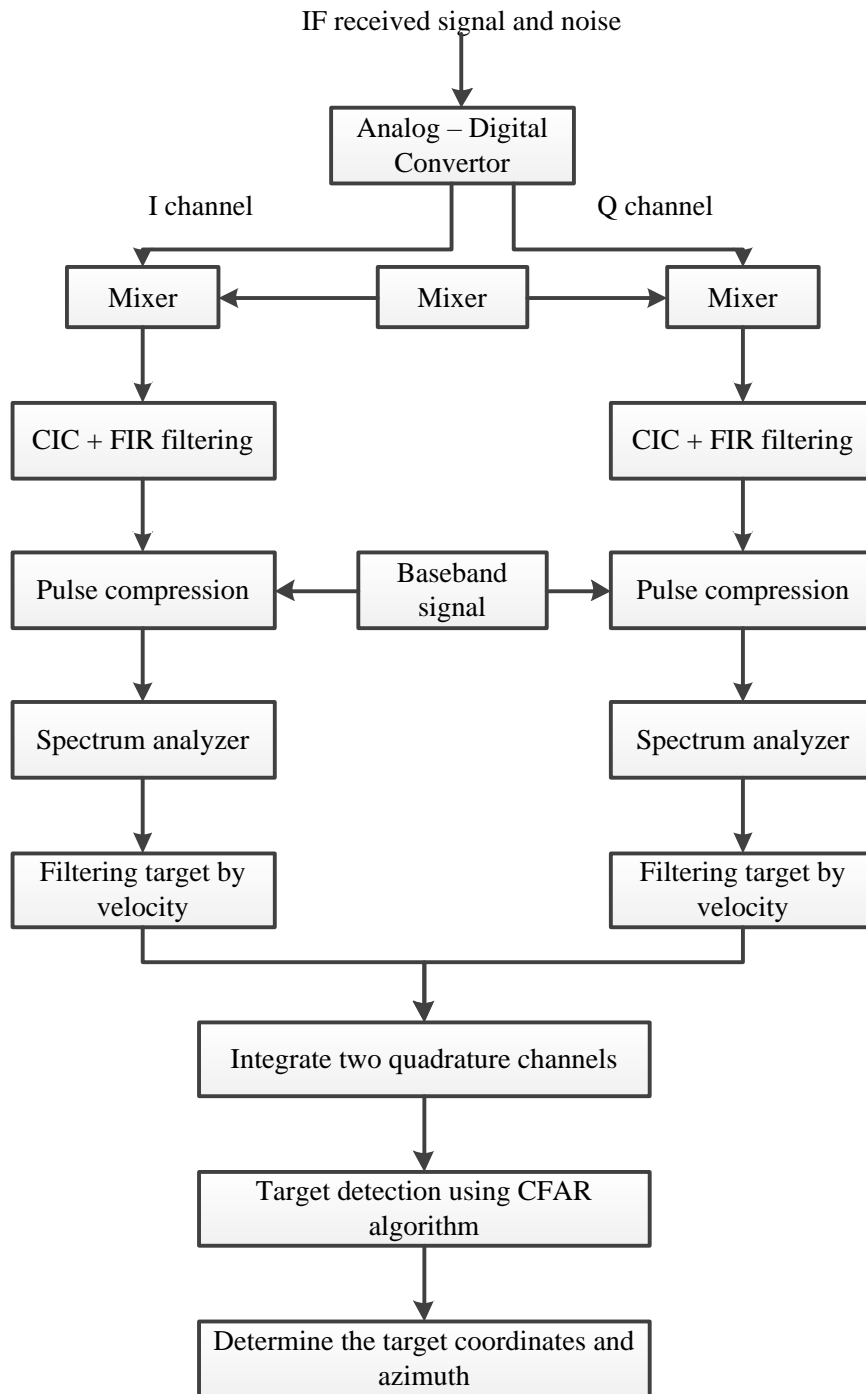


Figure 3. Structural diagram of the digital signal processing algorithm.

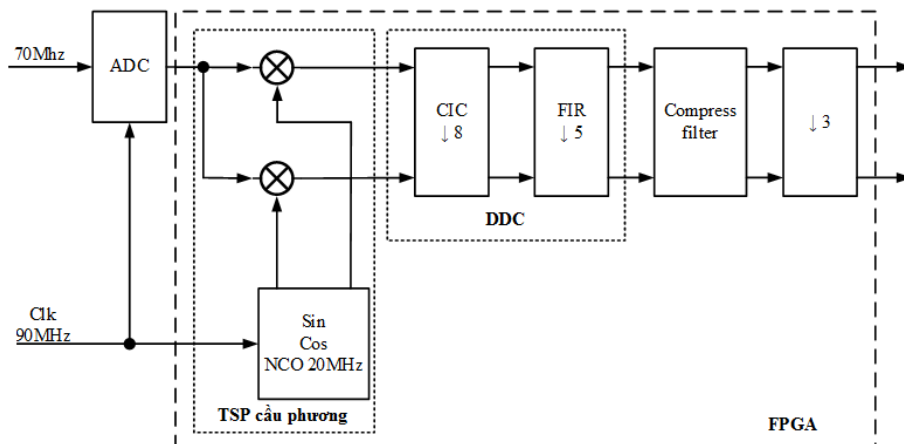


Figure 4. Structural diagram of the signal demodulation algorithm.

The technical solutions applied in the signal demodulation algorithm include:

- Reducing computational overload is achieved by using direct quadrature analog-to-digital conversion with a sampling frequency (90 MHz) that is less than twice the input signal frequency (undersampling method), combined with CIC filters in wideband signal demodulation (figure 4). The output signal from the multiplier is decimated in two stages: first, the signal passes through a CIC filter to eliminate harmonics of order 2 and above and is decimated by a factor of 8; then, it passes through an FIR filter and is decimated by a factor of 5. Consequently, after these two stages of filtering and decimation, the signal’s sampling rate is reduced from 90 MHz to 2.25 MHz before being fed into the signal compression filter. At the output of the compression filter, the energy is concentrated into a range bin, and the signal is further decimated by a factor of 3.
- Utilizing a Hamming-windowed FIR filter, which is an ideal weighted low-pass filter. The weighted coefficients $g_w(k)$ are obtained by modifying the coefficients of the non-windowed filter $g_{as}(k)$ with the window function $W(k)$. This approach allows the signal-to-noise ratio at the output of the compression filter to be improved by approximately 15 dB, while simultaneously reducing the sampling frequency by a factor of 5.
- Evaluating the target’s radial velocity using an optimal FIR comb filter whose frequency response approximates Chebyshev polynomials. The design of the low-pass filter set is optimal in that it minimizes the error between the desired frequency response and the actual frequency response.

3. TEST RESULTS

3.1. Test procedure

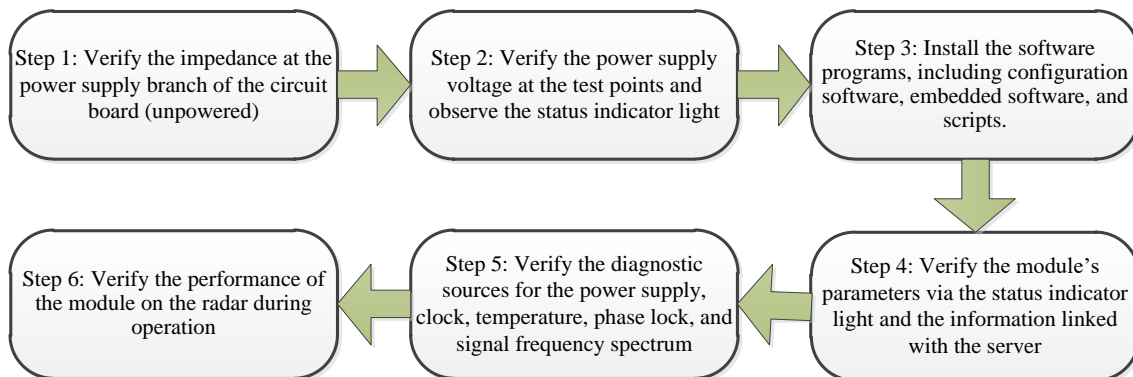


Figure 5. Testing and verification process.

The testing procedure for the circuit board, following the completion of the assembly process at the factory, is carried out in six steps (figure 5).

Install the software programs: Load the configuration file for the control FPGA, the "firmware" file, the hardware configuration data file for the control FPGA, the Linux operating system, and the plug-in scripts into the FLASH memory. To fully test the module's characteristics in the laboratory, the connection is performed as shown in figure 6.

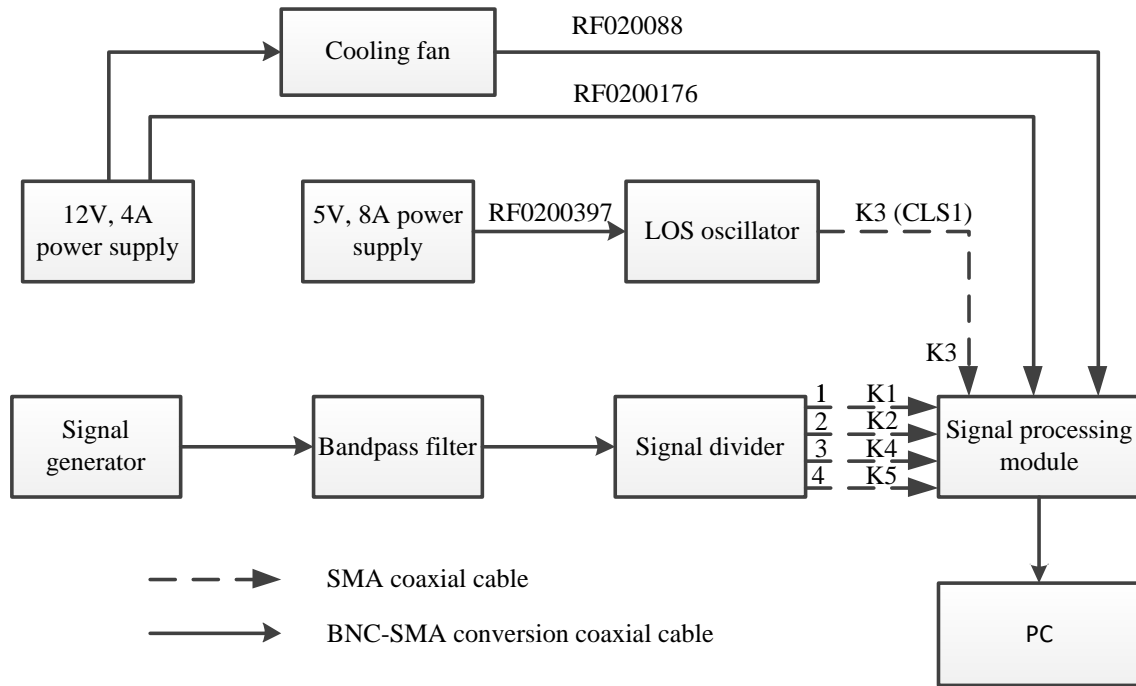


Figure 6. Connection diagram for testing module characteristics.

In figure 6, several measurement devices and support instruments are involved, including: a computer running Linux with dedicated test scripts, a USB-BLASTER programming cable, regulated power supplies of 12V/4A and 5V/8A, specialized module cables, an external oscillator board (LOS), a 1:5 power splitter, SMA coaxial cables, CAT 5E LAN cables, and a 70 MHz bandpass filter. The content, methods, and results of the tests are detailed in table 1.

Figure 1. Test results for some basic module characteristics.

Test content	Procedure	Test results	Evaluation
Testing the connection to the server	Connect the computer and module via LAN cable. At the computer, open a terminal (xterm) at \$RETIA_PROJECT/bin. Run the script ./dru_get_name.sh.	The script displays: #name "DRUID"	Connection successful
Power supply diagnosis	Run the script ./dru_get_volt.sh. in the terminal at (tj. \$RETIA_PROJECT/bin)	The script displays: #drudvolt "all" {0 0} "STE4V0" {3952 0} "STF5V5" {5472 0} ...	Nominal/measured value: 4V/3,952; 5V/5,472 No error warnings

Temperature measurement	Run the script <code>./dru_get_temp.sh</code> in a terminal at <code>\$RETIA_PROJECT/bin</code> .	The script displays: <code>#drudtmp "all" {0 0} "SRC"</code> <code>{313 0} "SRCA" {336 0}</code> <code>"SRCB" {311 0} ...</code>	Measured temps: 31.3 ⁰ ; 33.6 ⁰ ; 31.1 ⁰ ; No error warnings
PLL Frequency Lock (PLL)	Run the script <code>./dru_get_clk.sh</code> in a terminal at <code>\$RETIA_PROJECT/bin</code> .	Displays: <code>#name "DRUID" &</code> <code>#drudsig "all" {0 1} "CLS" {0 0}</code> <code>"VCSO" {0 0} "PLL" {0 0}</code> <code>"SYNC" {1 1} "COMMODO" {1 1}</code> <code>"ST6A" {0 0} "ST6B" {0 0}</code> <code>"ST6C" {0 0} "ST6D" {0 0}</code> <code>"ST6E" {0 0} &</code>	The phase-locked loop is frequency locked with no error warnings.

Figure 7 shows the measured input-output signal structure across the various functional stages, according to the structural diagram depicted in figure 4. Here, signals a and b are the LFM signal and the sine/cosine signals at the input of the quadrature phase demodulator; c is the output from the two quadrature channels; d is the output from the CIC filter; e is the output from the FIR filter; and f and g represent the input and output signals of the compression filter, respectively.

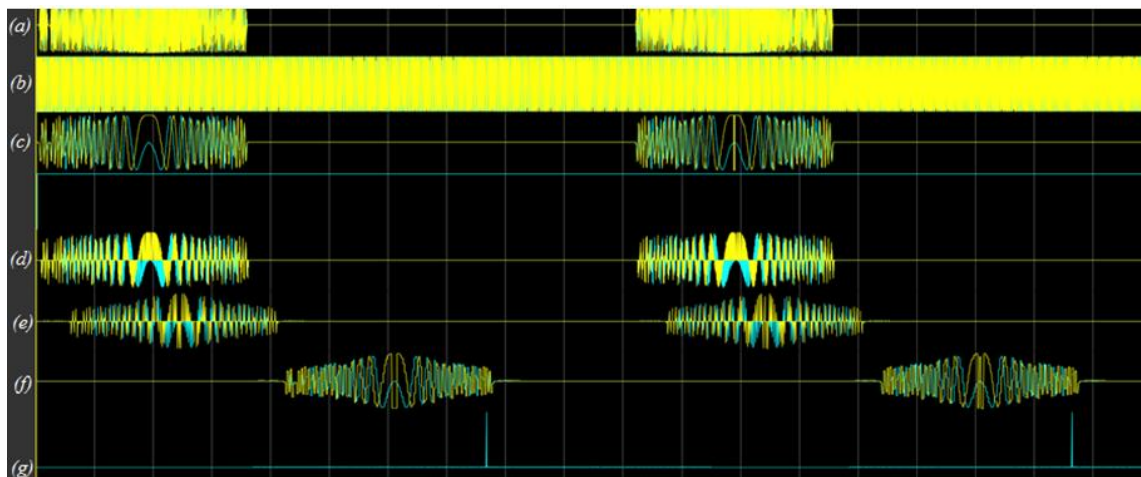


Figure 7. *Input-output signal structure of the functional blocks of the signal demodulation circuit.*

From the testing results, it is shown that:

- The phase characteristics of the signal remain undistorted when CIC and FIR filters are used for decimation.
- The signal’s amplitude envelope diminishes at higher frequencies, which leads to a degradation of the signal-to-noise ratio at the output of the compression filter. The degree of amplitude reduction at high frequencies is proportional to the decimation factor. To balance the decimation factor with an acceptable degradation in the signal-to-noise ratio, we chose a decimation factor of 120. A detailed explanation of this issue is provided in [1].

4. CONCLUSIONS

In the paper, the basis for selecting the signal processing algorithm, the hardware design solution, and the software development of the digital signal processing module for multi-channel linear frequency-modulated signals was analyzed. The applied solution group includes the use of

direct quadrature analog-to-digital conversion, decimation filtering, and optimal signal filtering to enhance the signal-to-noise ratio and reduce computational overload for the correlation compression filter. The research results confirm the research team's mastery of this new technology in the field. Through the research process and the application of advanced electronics and programming techniques, the authors have successfully integrated multiple hardware and software technologies to design and manufacture the digital signal processing module for multi-channel signals. The design and integration processes were carried out in a systematic and highly logical manner.

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TÓM TẮT

Nghiên cứu giải pháp kỹ thuật xử lý số tín hiệu nhằm nâng cao chất lượng thu của tổ hợp ra đa cảnh giới phòng không

Bài báo trình bày thuật toán xử lý tín hiệu, giải pháp thiết kế phần cứng và xây dựng phần mềm của mô-đun xử lý số tín hiệu ra đa điều tần tuyến tính nhằm tăng tỷ số tín/tạp, giảm quá tải tính toán số của hệ thống. Thuật toán xử lý tín hiệu được đề xuất thực hiện biến đổi tương tự số trực tiếp hai kênh cầu phương, lọc giảm mẫu, lọc tối ưu, lọc nén tương quan tín hiệu. Các linh kiện chức năng được lựa chọn có nhiều đặc tính ưu việt như hệ số tăng ích, tốc độ cao và không khan hiếm trên thị trường. Quá trình thiết kế phần cứng và xây dựng phần mềm được thực hiện theo quy trình khảo sát-mô phỏng-chế thử, có tính lô-gíc, hệ thống cao. Sản phẩm tạo ra được kiểm nghiệm thành công trên cả giá thử và đài ra đa.

Từ khóa: Xử lý số tín hiệu; Điều tần tuyến tính; Bộ lọc CIC; Bộ lọc FIR.