A double split-ring resonator based tunable filter for frequency detection and monitoring system

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ABSTRACT

This paper presents a compact, continuously tunable bandpass filter based on a double split-ring resonator (DSRR) loaded with two varactor diodes for modern wireless communication systems. The proposed design achieves a wide tuning range of 8 - 12 GHz (40% fractional bandwidth) through precise capacitance adjustment, addressing critical limitations of conventional tunable filters in bandwidth, reliability, and control complexity. By leveraging the DSRR's coupled resonance characteristics and independent varactor tuning, the filter maintains stable performance with return loss exceeding 10 dB across a 250-MHz passband. The architecture eliminates mechanical switches, offering improved reliability compared to MEMS/p-i-n diode alternatives while greatly reducing component count compared to traditional multi-bank filters. This work provides a foundation for developing reconfigurable RF front-ends that balance wide tunability, miniaturization, and power efficiency for 5G/6G and cognitive radio applications.

Keywords: Tunable filters; Double split-ring resonator; Frequency detection.

1. INTRODUCTION

The wireless communication industry is rapidly evolving to meet growing demands for multifunctional devices that support diverse applications, each requiring distinct frequency bands, operational modes, and bandwidths. Smartphones epitomize this trend, integrating technologies such as 4G, 5G, Bluetooth, and WiFi into a single compact platform. Concurrently, the push for miniaturization has become a dominant design paradigm, driving innovations in radio frequency (RF) front-end circuits to achieve smaller form factors without compromising performance. Filters, as critical components of these systems, must adapt to this trend while maintaining efficiency and versatility. Recent studies [1-4] highlight significant progress in miniaturized filter design, addressing the need for compact, reconfigurable solutions capable of supporting the expanding spectrum of wireless standards. This work aligns with these industry demands by exploring advanced filter architectures that balance miniaturization with multifunctional performance.

Conventional wireless systems typically employ fixed-frequency components, necessitating multiple passive elements to support multi-band operation, an approach that increases front-end complexity and size. Recent advances in tunable designs, including filters [5-18], couplers [19-21], and antennas [22], address this challenge through reconfigurable architectures that reduce component count while improving spectral efficiency. Early tunable filters utilized p-i-n or MEMS switches [5-7] to select discrete bands, but their mechanical limitations, reliability concerns, and added cost prompted exploration of alternative tuning methods.

Varactor-based designs [8-12] enabled continuous frequency agility, though with constrained tuning ranges. While multimode resonators [13-16] expanded bandwidth coverage, they often incurred trade-offs in insertion loss or physical size. Ferrite-based solutions [17, 18] achieved wide tuning (e.g., 5 - 19 GHz [18]), yet faced fabrication and cost barriers. These limitations highlight

the need for compact, reliable tunable filters with wide operational ranges, a critical requirement as RF systems transition to chip-scale integration. Current research prioritizes designs that balance extended tunability with simplified control mechanisms, aiming to advance next-generation wireless platforms without compromising miniaturization goals.

To address the limitations of existing tunable filters-including restricted bandwidth and complex control mechanisms - this work proposes a compact double split-ring resonator (DSRR) design integrated with two varactor diodes. The architecture enables continuous frequency tuning from 8 to 12 GHz through capacitance adjustment, achieving precise passband control without compromising performance stability. By combining wideband agility with a simplified tuning approach, this design advances frequency-selective solutions for spectrum monitoring and RF front-end systems. The study demonstrates how DSRR-based filters can reconcile wide tuning ranges (< 40% fractional bandwidth) with miniaturization goals, offering a scalable framework for reconfigurable wireless technologies. These contributions bridge critical gaps in adaptive filter design, supporting next-generation communication standards.

2. SYSTEM DESIGN

2.1. Block diagram

Figure 1 proposes a block diagram of the system, where the input signal is first filtered by a tunable band-select filter before being fed into a power detector (PD). The signal then goes through ADCs before entering a Field-Programmable Gate Array FPGA) for further processing.

Selecting a commercially available PD requires a high dynamic range and low-power measurement capability across the 8 - 12 GHz frequency range. The ADL5507 from Analog Devices (ADI) was chosen for its compliance with these specifications, including precise logarithmic detection and a broad operating bandwidth, as shown in table 1.

The proposed system is able to cover a frequency range of 8 – 12 GHz, with a wideband signal strength from – 30 dBm up to 0 dBm. The tunable filter can sweep over the range in 16 equal bands of 250-MHz bandwidth.

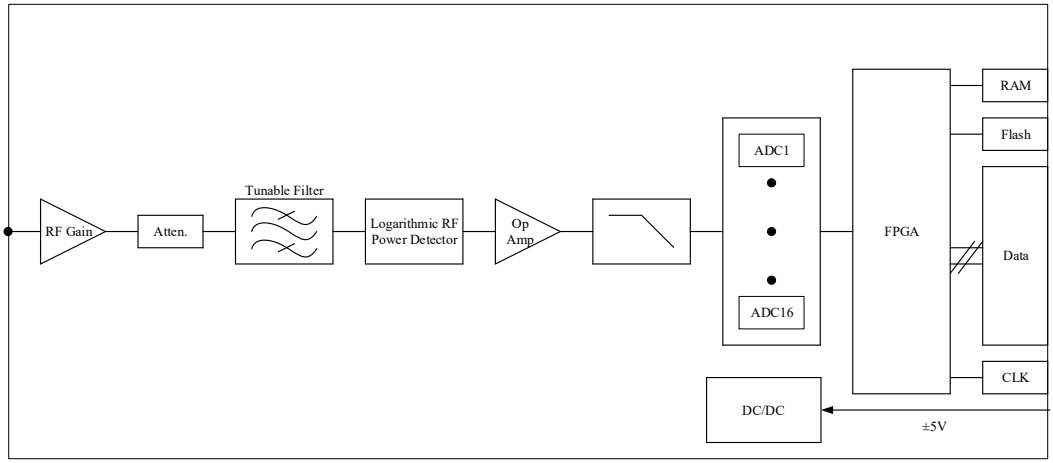


Figure 1. *Block diagram of the proposed frequency detecting system.*

Table 1. *Key specifications of ADL5507.*

Parameters	Value	Unit
Operating Frequency	10 – 1200	MHz
Min Input Power	-50	dBm
Max Input Power	-5	dBm
Power Detector Type	Logarithmic	

To ensure accurate frequency determination with an error of ≤0.65%, the tunable filter must exhibit a carefully controlled power-vs-frequency response, characterized by a flat passband and sharp roll-off. The response of the tunable filter should meet the requirements depicted in figure 2.

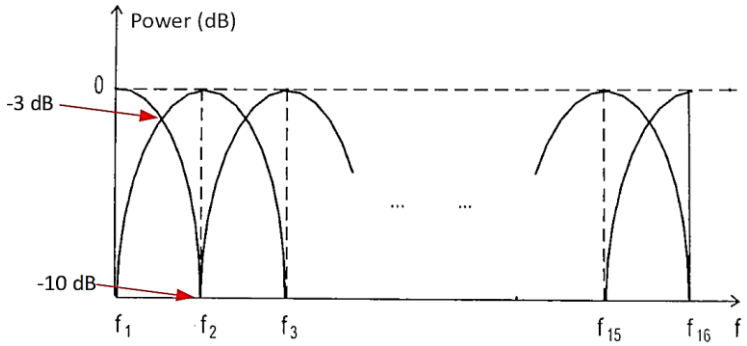


Figure 2. *Characteristic response of the tunable filter.*

2.2. FPGA algorithm

The system employs 16 ADCs, each of them configured to capture frequencies within a specific band (band 1 to band 16). To determine the input frequency, the ADC's values are compared to the threshold in order to determine the ones larger than the noise floor, as shown in figure 3. After the search, there are several results in which the ADC with the largest value identifies the band whose center frequency is closest to the input, while the second-largest ADC value reveals the input frequency's relative position.

In the second step, the FPGA identifies the group of consecutive values that satisfy the condition, i.e., larger than the noise floor, as shown in figure 4 (a). Gstart indicates the first element of the group, while Gnum represents the number of elements of the group. From the data from step 1 and step 2, the input frequency can be localized as follows. If the input frequency is higher than the center frequency of the band corresponding to the largest ADC, the second-largest ADC value will belong to the subsequent band (e.g., Band N+1); Conversely, if lower, it will correspond to the preceding band (e.g., Band N−1).

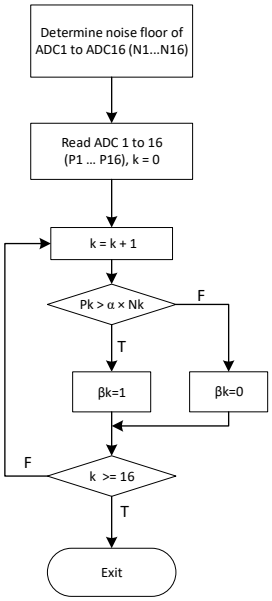


Figure 3. *Determining ADC's power values more than threshold in comparison with noise floor βk = 1 means that RF input may be in bank k.*

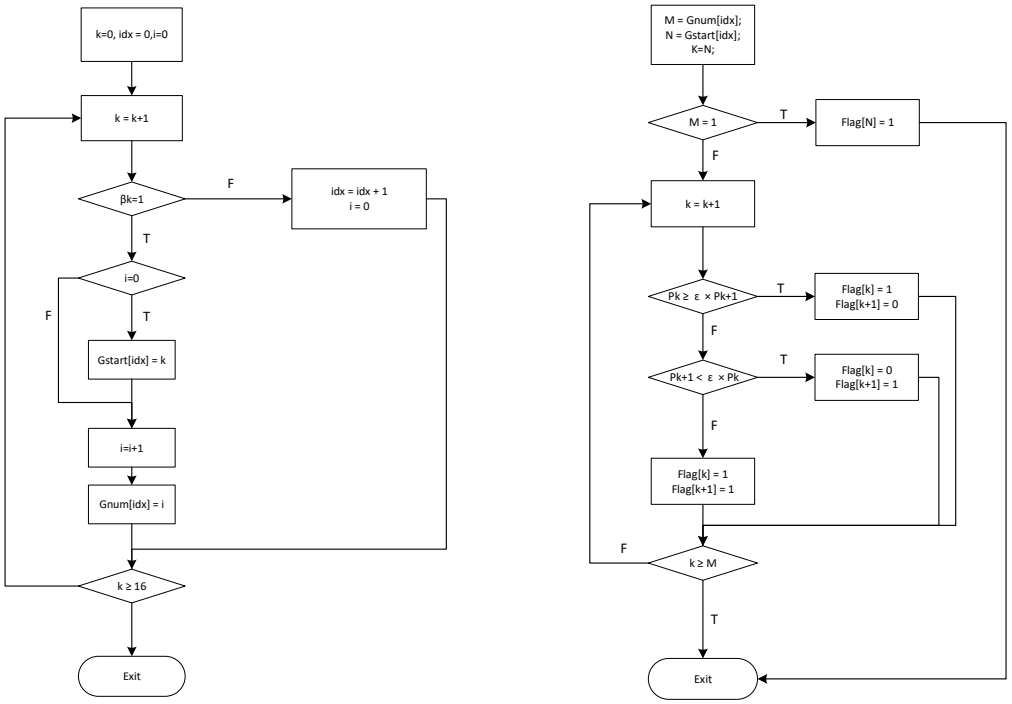


Figure 4. *(a) Determining the Group of consecutive power values that are more than the Noise Floor; (b) Check each group's Power value of step 2 to avoid power values of the bank boundary (ε is a threshold that depends on the filter's response. Flag[k] = 1 means that the value is identified at bank k frequency in the RF input).*

In cases where two adjacent ADCs yield equal values, the input frequency lies exactly midway between their respective center frequencies. To avoid this confusion, the third step is introduced to the FPGA depicted in figure 4 (b). This step checks the results from previous steps to identify values at the bank boundary.

For example, as illustrated in figure 5, an input frequency triggering ADC5 as the largest and ADC6 as the second-largest indicates that the signal lies near Band 5's center frequency but is slightly higher. Calibration data then refines this estimate to pinpoint the exact input frequency within the resolved band.

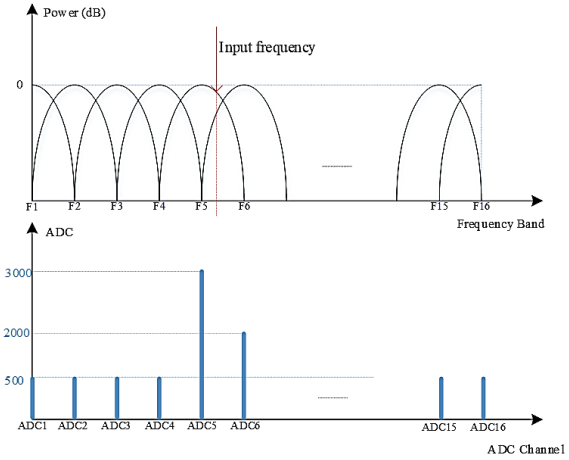


Figure 5. *The position of input frequency in the system and the ADCs' corresponding values.*

3. TUNABLE FILTER DESIGN

3.1. Equivalent circuit and analysis

The filter topology employs a DSRR, shown in figure 6, due to its superior tuning capabilities. The DSRR's dual-slot structure enables independent loading of varactor diodes into each ring, providing enhanced tuning resolution and a wider frequency range compared to single-ring designs. This multi-parameter control allows precise adjustment of both the inner and outer ring resonances. By loading varactors into the DSRR slots, the filter achieves dynamic reconfiguration tuning C_1 and C_2 modifies the coupling and resonant frequencies, enabling tunable band selection. The DSRR's geometry ensures that C_1 and C_2 can be optimized separately, offering finer control over the filter's passband characteristics (e.g., center frequency and bandwidth) while maintaining compact dimensions. This approach combines the DSRR's inherent frequency selectivity with the agility of varactor-based tuning, making it ideal for applications requiring high frequency resolution.

The DSRR's electrical behavior can be modeled using the equivalent circuit depicted in figure 7 (a). In this representation, C_c denotes the coupling capacitance between the (DSRR) and the input and output transmission lines. The intrinsic inductance of the DSRR, L_r, arises.

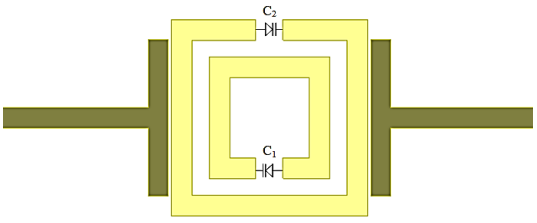


Figure 6. *The double split-ring resonator (DSRR) loaded with varactors.*

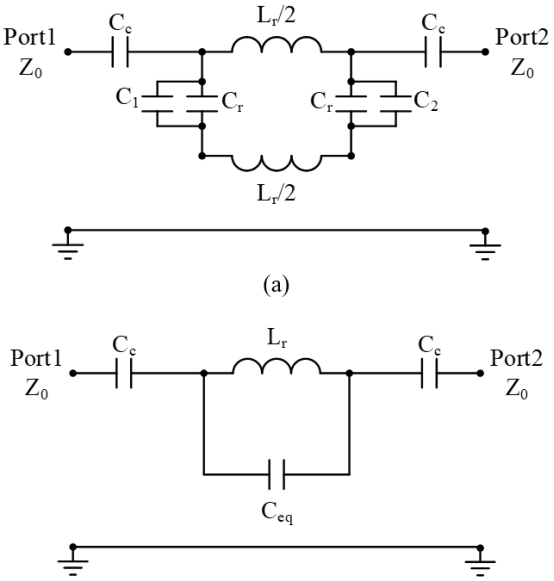


Figure 7. *(a) Equivalent circuit of the DRSS and (b) its simplified model.*

From the metallic ring structure, while C_r represents the inherent capacitance of the split rings, collectively determining the resonant frequency, the simplified equivalent circuit reduces the analysis of the filter's frequency response and tuning range while preserving the physical insights of the DSRR's electromagnetic behavior. The C_{eq} is calculated by equation (1) in terms of C_1, C_2, C_r.

$$C_{eq} = \frac{(C_1 + C_r)(C_2 + C_r)}{C_1 + C_2 + 2C_r} \tag{1}$$

In the proposed filter design, the optimal values for the inductors and capacitors are determined through a systematic approach. This involves ensuring that the design satisfies essential criteria: perfect impedance matching and achieving a maximum signal transfer from one port to another.

The scattering parameter can be calculated with the derivation of the network's ABCD transmission matrix (A-matrix), as illustrated in the following analysis. This foundational step enables systematic determination of the filter's characteristics through matrix transformation techniques.

$$[ABCD] = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{j\omega C_c} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & j\left(\omega L_r - \frac{1}{\omega C_{eq}}\right) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{j\omega C_c} \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & \frac{2}{j\omega C_c} + j\left(\omega L_r - \frac{1}{\omega C_{eq}}\right) \\ 0 & 1 \end{bmatrix} \quad (2)$$

Hence, the S_{11} and S_{21} can be obtained using formulas in [23] as below:

$$S_{11} = \frac{j(\omega L_r - \frac{1}{\omega C_{eq}} - \frac{2}{\omega C_c})}{j\left(\omega L_r - \frac{1}{\omega C_{eq}} - \frac{2}{\omega C_c}\right) + 2Z_0} \quad (3)$$

$$S_{21} = \frac{2Z_0}{j\left(\omega L_r - \frac{1}{\omega C_{eq}} - \frac{2}{\omega C_c}\right) + 2Z_0} \quad (4)$$

Solving equations (3) and (4) establishes the relationship between C_1, C_2, C_r, and L_r. Based on these relationships, appropriate values for L_r and C_r are selected to determine the physical dimensions of the unloaded DSRR.

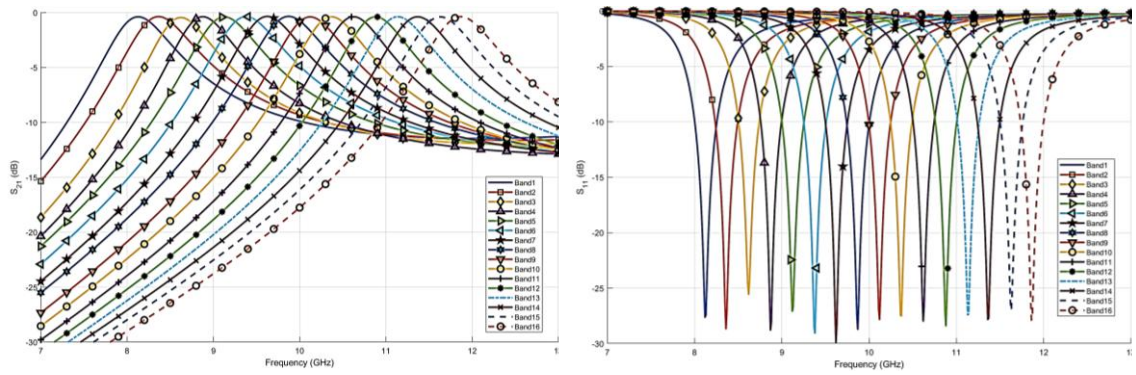
3.2. Design procedure

The proposed filter design methodology follows a structured four-stage approach:

- Specification Definition: Critical performance requirements, including tuning range (8 - 12 GHz) and port impedance (Z_0), are established.
- Resonator Synthesis: Equations (3) and (4) are employed to derive the DSRR geometric parameters.
- Loading Calculation: The loaded values of varactor capacitance of C_1 and C_2 through analytical solutions of (3) and (4).
- EM Simulation: Varactor models (representing C_1 and C_2) are incorporated into full-wave electromagnetic simulations, validating performance against initial specifications.

3.3. Simulation results

The tunable filter design is simulated in ANSYS HFSS to analyze its electromagnetic performance. Figure 8 depicts the S-parameter responses ($|S_{21}|$ and $|S_{11}|$) across the tuning range, demonstrating multiple bandpasses in the range of 8 – 12 GHz. The simulated results meet all target specifications, including a consistent 250-MHz bandwidth across tuning states. Excellent agreement is observed between the predicted and required frequency responses, validating the design methodology.



(a) *(b)*

Figure 6. *Tunable filter's (a) insertion loss and (b) return loss.*

Table 2 summarizes the bandpass of the tunable filter, provided that its return loss is better than 10 dB, along with the loading values of C_1 and C_2 from the loaded varactors.

Table 2. *Simulated bandpass corresponding to loaded values of varactors' capacitance.*

Band	Frequency (GHz)	C_1 (pF)	C_2 (pF)
1	8.00 – 8.26	0.32	5.70
2	8.24 – 8.50	0.43	5.70
3	8.50 – 8.74	0.47	5.70
4	8.76 – 9.00	0.58	5.90
5	9.00 – 9.25	0.80	6.30
6	9.25 – 9.51	1.18	6.30
7	9.5 – 9.75	2.03	6.80
8	9.74 – 10	2.24	7.20
9	10.00 – 10.25	2.71	7.60
10	10. 25 – 10.49	3.89	7.70
11	10.50 – 10.75	4.10	7.90
12	10.76 – 11.00	4.14	8.10
13	11.01 – 11.26	4.35	9.00
14	11.24 – 11.50	4.57	9.30
15	11.50 – 11.76	4.81	9.30
16	11.74 – 12.00	4.98	9.60

4. CONCLUSIONS

This paper introduces a tunable bandpass filter design utilizing a DSRR loaded with two varactor diodes. By adjusting the varactors' capacitance values, the filter achieves continuous frequency tuning across an 8 - 12 GHz range, enabling precise control over its passband characteristics. The proposed architecture offers a compact and efficient solution for frequency-selective applications, particularly suited for spectrum monitoring and frequency detection systems. Its ability to maintain consistent performance while sweeping across a wide bandwidth underscores its practicality for modern RF systems. This work provides a foundation for developing reconfigurable filters with adaptable frequency responses to meet evolving communication demands.

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TÓM TẮT

Bộ lọc thông dải có thể tùy chỉnh sử dụng cấu trúc cộng hưởng hai vòng hở ứng dụng trong hệ thống phát hiện và theo dõi tần số

Bài báo này đề xuất một bộ lọc thông dải có thể tùy chỉnh liên tục, nhỏ gọn dựa trên cấu trúc cộng hưởng hai vòng hở (DSRR) tích hợp hai đi ốt varactor nhằm ứng dụng trong các hệ thống thông tin liên lạc hiện đại. Thiết kế này có thể tùy chỉnh được trên một dải tần số rộng từ 8 – 12 GHz (40% băng thông tỷ lệ) nhờ vào việc tinh chỉnh các giá trị điện dung của đi ốt giúp cải tiến các cấu trúc bộ lọc tùy chỉnh thông thường về mặt băng thông, độ ổn định và độ phức tạp điều khiển. Nhờ cấu trúc DSRR, bộ lọc đảm bảo độ phối hợp trở kháng tốt hơn 10 dB trong 250-MHz băng thông trên toàn dải tần hoạt động. Kiến trúc này loại bỏ yêu cầu về số lượng thành phần đi kèm dù vẫn đảm bảo độ ổn định so với các cấu trúc sử dụng MEMS/p-i-n đi ốt. Thiết kế này tạo tiền để cho các thiết kế sau này cho các hệ thống 5G/6G trong tương lai.

Từ khoá: Bộ lọc thông dải có thể tùy chỉnh; Cấu trúc cộng hưởng hai vòng hở; Phát hiện tần số.