Enhancing performance of GaN MMIC power amplifiers through transistor sizing and bias voltage optimization

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ABSTRACT

The paper presents a method for optimizing bias voltage and transistor size to improve power conversion efficiency (PAE) and output power in high-power amplifiers using GaN MMIC technology. Using simulation with the MP2500S transistor model in the WIN NP25 technology library on ADS software, the paper analyzed the effects of different V_{GS}, V_{DS} voltage levels and gate sizes on PAE, output power and Gain. The simulation and analysis results are applied to satellite communication uplink amplifiers (14 GHz ÷ 14.5 GHz) with gate width configurations from 2×75 µm to 8×125 µm. The results show that, with appropriate gate width, the selection of bias point in AB mode can significantly improve PAE while still ensuring the required P_{out}. However, the study also shows that excessive gate width expansion can reduce performance due to the trapping effect, parasitic leakage current and self-heating effect. The paper proposes a method to investigate and select the optimal transistor size and bias voltage in GaN PA design, particularly for Ku-band applications (12÷18 GHz) requiring high power and efficiency. This study contributes to improving the performance of GaN HEMT in power electronics applications.

Keywords: GaN HEMT; Gate width; Bias voltage; Power amplifier; Ku_band; WIN NP25; Loadpull.

1. INTRODUCTION

GaN HEMT (High Electron Mobility Transistor) is an advanced semiconductor technology for designing *monolithic microwave integrated circuit power amplifiers* (*MMIC PAs*) due to its ability to operate at high voltages, high current densities, and high frequencies. With superior breakdown voltage and thermal efficiency compared to Si or GaAs technology, GaN HEMT enables the design of power amplifiers with high output power, high efficiency, and compact size, making them particularly suitable for radar, satellite communications, and high-power communication applications.

Ku-band monolithic microwave integrated circuit (MMIC) power amplifiers (PAs) are mainly designed using 0.25 µm or 0.15 µm gallium nitride (GaN) technology with three or four-stage structures. The number of final stage transistors can be 4, 8, 16, 32, or 64 to achieve the desired large output power [1, 2]. In these multi-stage power amplifiers, the first stage amplifier requires a large gain. The subsequent stages create a sufficient input power level for the final stage, which is responsible for generating the necessary high-power output. To improve uniform performance with a wide input signal range, use Dorherty-type amplifiers [3] or F-mode amplifiers.

The gain, output power, and efficiency of GaN HEMT transistors depend strongly on tube geometry, particularly total gate width. Optimizing these dimensions affects not only amplifier performance and output power but also factors such as heat dissipation, linearity, and device reliability [4]. Additionally, the bias voltage determines the transistor's operating mode, greatly affecting the amplifier circuit's linearity and performance.

In the context of the increasing demand for high-power and high-performance electronic systems, studying and selecting the optimal bias voltage and dimensions for GaN HEMTs is urgent. This paper aims to analyze the impact of transistor dimensions on efficiency and output power to propose appropriate design guidelines for practical applications. By analyzing simulation results, this study will reveal the relationship between geometric parameters and the performance of GaN HEMTs, thereby improving the efficiency of power system design. At the same time, it will evaluate the effects of bias voltage on amplifier circuit performance.

This paper is further structured into four sections as follows: Section 2 - Theoretical basis; Section 3 – Simulation setup; Section 4 - Simulation results and discussion; Section 5 - Conclusions.

2. THEORETICAL BASIS

GaN HEMT is a non-polarized N-channel semiconductor device that typically operates in depletion-mode (normally-on), meaning that even when no voltage is applied to the gate, the 2D electron gas (2DEG) channel (figure 1) remains between the source and drain, allowing natural current flow, and the device remains in its default "on" state. This characteristic originates from the AlGaN/GaN heterostructure, where the charge asymmetry caused by spontaneous polarization and piezoelectric polarization in the AlGaN layer creates a fixed charge layer at the AlGaN/GaN interface, pulling electrons to accumulate on the GaN surface to form the 2DEG channel even when $V_{GS} = 0$. This is the fundamental difference between GaN HEMTs and Si MOSFETs, which require a positive $V_{GS} > V_{th}$ to attract charge and form a conduction channel. To turn off the current, a negative gate voltage relative to the source must be applied, creating a reverse field that pushes electrons out of the 2DEG channel, eliminating conduction, thereby cutting off the current [1]. The value of V_{GS} required to initiate this current cutoff is the threshold voltage V_{th} , and since a negative voltage must be applied to turn off the channel, the Vth of GaN HEMTs is typically negative. The linear and nonlinear operating models of the transistor are characterized by the following key parameters: The threshold voltage (V_{th}) typically ranges from -2.5 V to -3 V. The voltage $V_{DS,max}$ can reach nearly 100 V, enabling operation at high power levels with good breakdown voltage performance. The maximum drain current $I_{ds,max}$ is linearly proportional to the total gate width $W_{g,tot}$ according to the expression:

$$I_{ds,max} \approx J_{sat} \cdot W_{g,tot} \tag{1}$$

Where: - J_{sat} is the saturation current density (typically 0.8–1.2 A/mm for GaN HEMTs) [2];
- $W_{g,tot}$ is the total gate width (sum of parallel fingers).

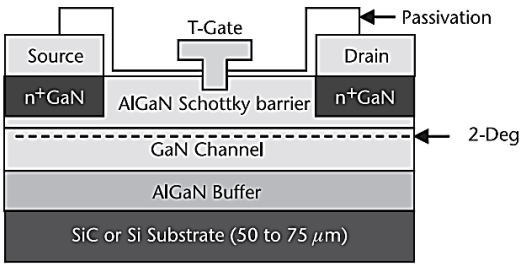


Figure 1. *GaN device structure [2].*

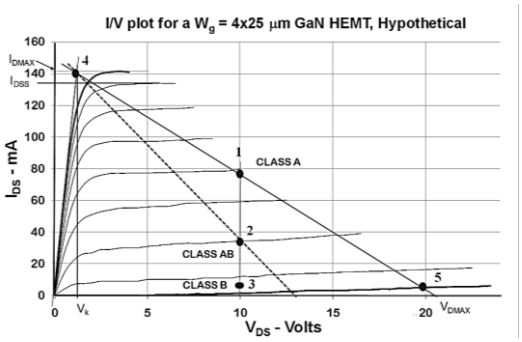


Figure 2. *I-V characteristics of GaN HEMT with $W_g = 4 \times 25$ μm, $L_g = 0.125$ μm for $-3.5 \leq V_{gs} \leq 0$, step of 0.5 V [2].*

The bias voltage (I_{DS}) is determined by V_{GS} and V_{DS} which determines the operating mode of the transistor (Class A, AB, B, C) (figure 2). The maximum output power of the circuit can be

achieved in Class A mode, approximately estimated from the optimal load line according to equation (2). However, in Class A mode, the efficiency achieved is low, with the maximum PAE always less than 25% (according to equation (4)). To balance efficiency, output power, and linearity, the transistor is typically biased in Class AB mode. However, the degree to which they are biased closer to A or B is a matter of consideration.

$$P_{out,\max} = \frac{1}{8}.V_{DS,\max}.I_{DS,\max} \tag{2}$$

$$P_{DC} = V_{DS}.I_{DS} \tag{3}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}.100\% \tag{4}$$

$$Wg,tot = NOF * UGW \tag{5}$$

The total gate width ($W_{g, tot}$), determined by equation (5), determines the transistor's current-carrying capacity, thereby affecting the maximum power. To increase $W_{(g, tot)}$, one can increase UGW or increase NOF. Increasing the gate size increases the transistor's current conduction ability, thereby increasing the maximum power and gain. However, as the gate size increases, the parasitic effect also increases. This reduces the maximum frequency according to expression (6). Additionally, the active area increases, and the number of surface traps increases. This increases the trapping phenomenon at the energy levels inside the material or at the interface. This causes effects such as reducing the I_{DS} current when V_{DS} increases (figure 3). It also causes nonlinear distortion and performance degradation [6].

$$f_{\max} = \frac{f_T}{2\sqrt{g_{ds}\left(R_g + R_s\right) + 2\pi f_T R_g C_{gd}}} \tag{6}$$

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{7}$$

In which, gm - Transconductance; C_{gs}, C_{gd} - Parasitic capacitance; R_g, R_s - Parasitic resistance.

Thus, in the design of MMIC PAs, bias voltage and total gate width are important design parameters because they directly affect the operating mode, operating frequency range, gain, output power and PAE conversion efficiency. The relationship between bias voltage, gate width and circuit performance can be analyzed through load-pull simulation to help determine the optimal load impedances (Z_L) at each configuration. As a result, it is possible to find the bias voltage/gate width parameter pair that gives the best circuit performance.

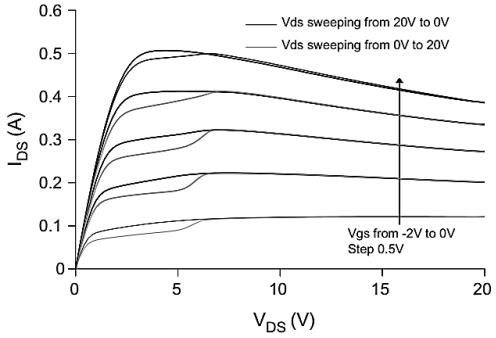


Figure 3. *Trapping effect [3].*

3. SIMULATION SETUP

The survey and evaluation method is carried out in 2 directions:

- Evaluate the influence of transistor size on small signal parameters, including stability factor K, maximum amplification factor (MAG), large signal parameters: output power, amplification factor, PAE.

- Evaluate the influence of bias voltage on amplifier circuit performance at a size selected from the above step.

The simulation is performed using ADS software and the GaN HEMT MP2500S transistor model from the Win Semiconductors PDK NP25XX library.

- Evaluate the influence of size:

+ Choose size from small, to medium, to large: 2x 75 µm; 2x 125 µm; 4x 125 µm; 6x 125 µm; 6 x 150 µm; 8x 125 µm.

+ Perform S-param simulation from 1 GHz to 60 GHz to evaluate small signal parameters with V_{DS} = 28 V, V_{GS} = (-2.6 ÷ -1.8) V.

+ Simulate Loadpull, Sourcepull to find $Z_{L,\,opt}$ and $Z_{S,\,opt}$ corresponding to each size at frequency f = 14.25 GHz. The optimal impedance values are the intersection of power-contour and PAE-contour, optimized for high output power while ensuring good PAE performance.

+ Simulate HB with Pin from 0÷29 dBm at the same bias value V_{GS} = -2.4 V and V_{DS} = 28 V, set as figure 4.

- Evaluate the influence of bias voltage at one size. Circuit configuration:

+ Sweep V_{GS} (-2.6 V → - 1.8 V), V_{DS} = 28 V;

+ Sweep V_{DS} (28 V → 36 V), V_{GS} = -2.4 V.

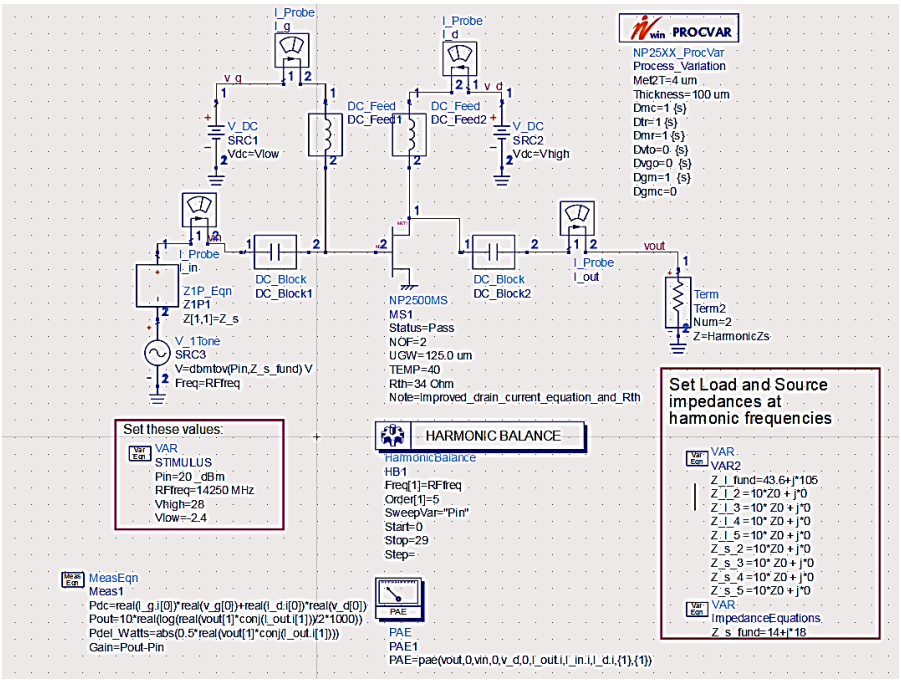


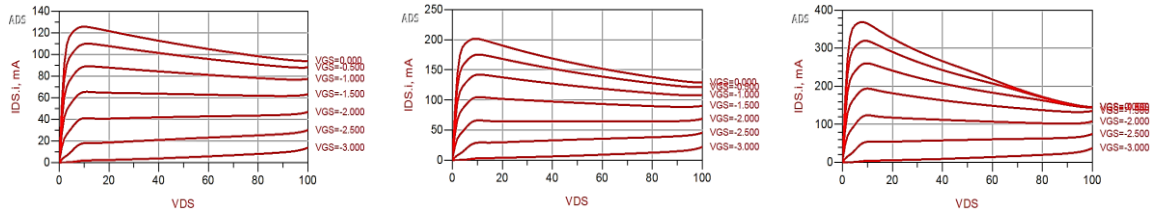
Figure 4. *Simulation setup for evaluating the performance of PA with different transistor sizes.*

4. SIMULATION RESULTS AND DISCUSSIONS

4.1. Transistor size and trapping effect

The trapping effect was evaluated by varying the size of the transistor, as shown in the I-V simulation results with different device sizes, as in figure 5. The results show that $V_{DS,\,max}$ of the

transistor can reach nearly 100 V, with V_{th} ~ -3 V. At a size of 2 x 75 µm, the trapping effect is minimal, but when the size increases to 4 x 125 µm, the effect becomes very pronounced. The choice of load must be appropriate to prevent the trapping effect from distorting the signal, which would affect $P_{out, max}$ and PAE of the circuit.



a) 2x75 µm. *b) 2x125 µm.* *c) 4x125 µm.*

Figure 5. *Trapping effect when changing transistor size.*

4.2. Selection of transistor size

This section's selection analysis will focus on designing a power amplifier circuit in the 14÷14.5 GHz frequency range as an example. According to the simulation results in figure 6, the stability factor K is low in the Ku region for sizes 2x75 to 4x125. Thus, an active stabilization network is needed. At 6x125 µm, K ≈ 1 at 14 GHz (thin margin). The circuit is sensitive to bias and temperature, and adding a real matching network can achieve K < 1. At 6x150 µm, K > 1 in the 14-14.5 GHz region, with a good safety margin, and the K line has no deep bottom near 2fo. There is little risk of out-of-band oscillation after circuit coupling. With 8x125 µm, there is a deep bottom K around 18÷25 GHz, and out-of-band oscillation is likely to occur. Thus, as the size increases up to a certain limit, the stability factor increases; However, further increases in size cause large parasitic losses, making the circuit more susceptible to oscillation. Additionally, as the size increases, the amplification factor decreases, as does f_{max} (the frequency at which MaxGain = 0 dB) (figure 7). However, for working frequencies approaching the Ku band, the large f_{max} is still satisfactory. To balance the stability and amplification factors, it is recommended to use 6 x 150 µm for the final power stage, 4x125 µm or 6x125 µm for the driver stage, and 2 x 125 µm for the first stage, combined with a stabilization circuit to achieve a higher amplification factor.

Using the optimal impedance values for Pout and PAE corresponding to different transistor sizes, we found that increasing the size increases the saturation power and gain. However, PAE gradually decreases with size when Pin is small because the increase in Pout is insufficient to compensate for the increase in P_{DC} (table 1).

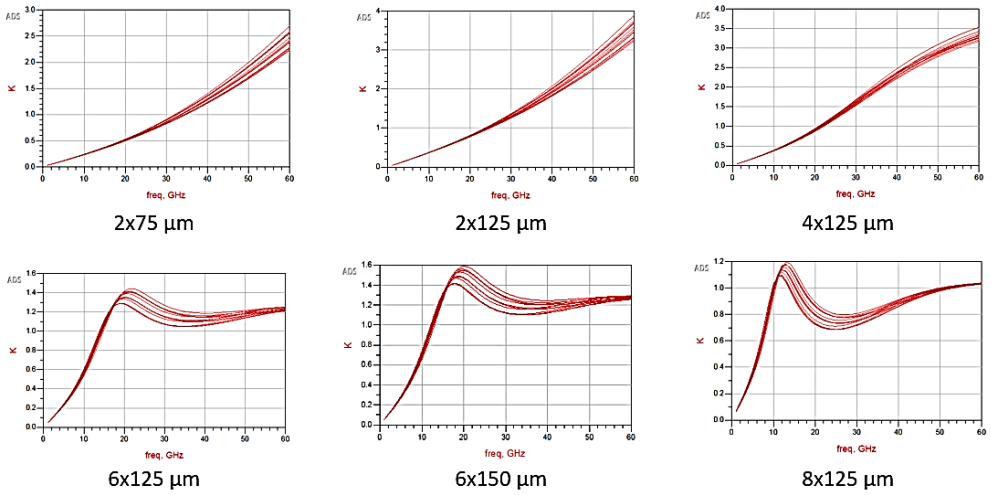


Figure 6. *Stability vs size and bias voltage V_{GS} (- 2.6 V ÷ - 1.8 V); V_{DS} (28 V ÷ 36 V).*

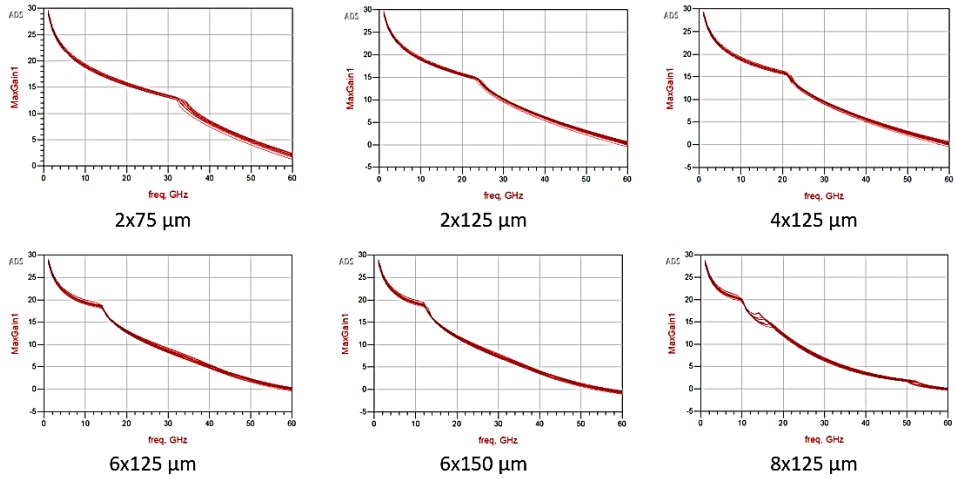


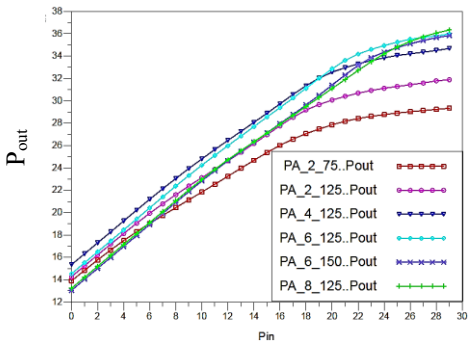
Figure 7. *Maximum available gain (MAG), fmax vs size and bias voltage.*

Table 1. *Power Dissipation P_{DC} vs the size of the transistor.*

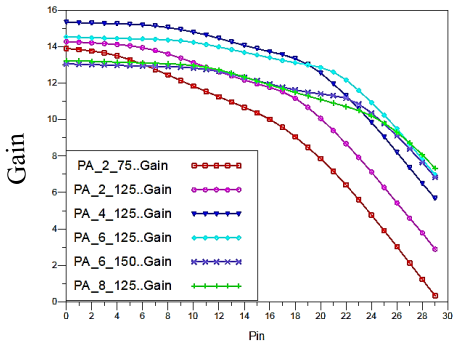
Size	2x75	2x125	4x125	6x125	6x150	8x125
P_{DC} (W)	0.662	1.053	1.889	2.564	2.876	3.115

When Pin ≤ 18 dBm and the size increases from 2x75 to 4x125, Pout and gain gradually increase, and PAE gradually decreases, but not by much. At this small input level, the larger size yields lower performance than 4x125 for all three parameters.

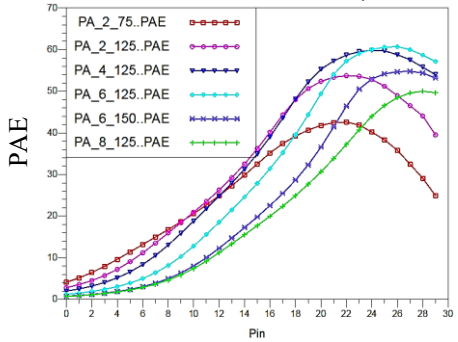
At $P_{in} \geq 15$ dBm, Pout, gain, and PAE increase significantly when the size increases from 2x75 to 4x125. This is because the small size saturates earlier; the output power approaches the saturation value, and the large input power helps the larger tubes work more effectively in the conduction region.



a) P_{out} vs P_{in}, size of transistor.



b) Gain vs P_{in}, size of transistor.



c) PAE vs P_{in}, size of transistor.

Figure 8. *Simulation results evaluating PA performance when the transistor size changes.*

When $P_{in} \geq 18$ dBm, the 6x125 has a higher power output and gain than the 4x125, but a lower power-added efficiency (PAE) until Pin ≥ 24 dBm. Then, the PAE of the 6x125 is better than that of the 4x125. This is due to the trapping effect, as well as the parasitic resistance, which increases as the number of fingers increases from 4 to 6. Although the 6x125 μm configuration has a larger total gate width, which results in a higher saturation current potential, an increase in current density and local temperature in the fingers can degrade amplifier efficiency, which reduces output power at certain input power levels. The 4x125 configuration approaches saturation only when $P_{in} \geq 24$ dBm, so the PAE drops lower. The 6x150 and 8x125 sizes perform worse than the aforementioned sizes only when $P_{in} \geq 23$ dBm. In this case, Pout and Gain are close to those of the 6x125, but the PAE is worse due to the large P_{DC}. This is due to the large-size trapping effect and large parasitic resistance, which cause a large loss.

Depending on the position of the transistor in the first or last amplifier stage and the input power range, the article suggests choosing the size. Size 2x75 has a small Pout and gain, so it is not used. The first amplifier stage usually has an input power of $P_{in} \leq 18$ dBm. If a high amplification factor is desired, use size 4x125. For the next amplifier stage with Pin ≥ 18 dBm, choose size 6x125 because it has better stability and linearity and a higher Pout with a balance between gain and PAE.

In addition, an important factor to consider when choosing the size of the transistor is the impedance value that the matching circuit must match. Figure 9 is the optimal load impedance and the optimal source that must be matched to achieve the Pout, Gain, and PAE criteria analyzed above. Impedances closer to the center are easier to match, resulting in wider matching and lower loss. On the contrary, points located further from the center, especially near the edge of the diagram, require a more complex matching circuit, increasing the conduction loss and narrowing the effective bandwidth [7]. A complex impedance matching circuit will lead to an increase in chip size, which greatly increases the chip cost. The results in figure 8 are evaluated with the optimal impedance value, and these results are degraded more in practice if the impedance value is difficult to match. This is a factor to consider when choosing the transistor size to balance the performance, output power, and practicality of a simpler, more efficient matching circuit.

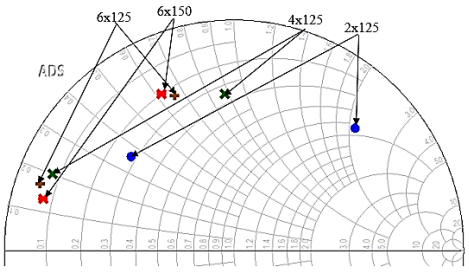
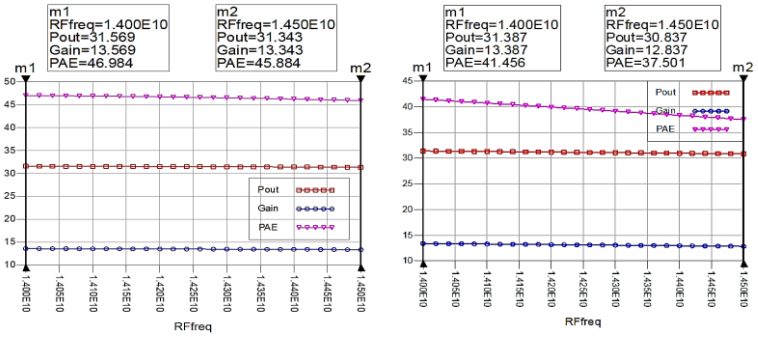


Figure 9. *$Z_{L,\,opt}$, $Z_{S,\,opt}$ vs different sizes of transistor.*

Based on the simulation results, it can be seen that the 2x125 option is easy to perform impedance matching and achieves better power and efficiency, so it is a good choice for amplifiers that require a wide bandwidth. With the size of 4x125, the Z_{Lopt} resistor is relatively close to the center, easy to match. Z_{Sopt} is further away but provides better Pout, PAE, and linearity, so it is a good choice for high-power amplifiers. The 6x125 and 6x150 structures have quite close impedances, so between these two sizes, other factors should be compared as in the previous section.

As expected, as the size increases, the parasitic values increase, and the optimal impedance, according to the transistor sizes, depends more on the frequency. As shown in figure 10, the 4x125 size has a smaller difference at the beginning and end of the frequency band compared to the 6x125 size. Specifically, ΔP_{out} and ΔGain are 0.226 and 0.55, respectively; ΔPAE is 1.1 and 3.995, respectively. This assessment is based on a narrow frequency band. A more accurate assessment of a wider band is made by surveying many frequency points and choosing the average value. Thus, when choosing the transistor size, this factor should be considered as well.



a) 4x125 µm @ P_{in} = 18 dBm. *b) 6x125 µm @ P_{in} = 18 dBm.*

Figure 10. *Performance of PA over a frequency band vs difference sizes of transistors.*

4.3. Selection of bias voltage

Evaluate the influence of the bias point with a transistor size 4x125 µm.

Based on the previous recommendation, the 4x125 size is recommended for use with $P_{in} \leq 18$ dBm. In this Pin region, when increasing V_{GS}, Pout, Gain both increase, linearity increases, and PAE decreases because P_{DC} increases proportionally with V_{GS}. With V_{GS} = -2.6 V, AB mode near B, gain is smaller and quickly decays, poor linearity, in the $P_{in} \geq 10$ dBm region, PAE benefits but is insignificant. Thus, choosing high V_{GS} brings high power, good linearity, but reduces PAE and high gate voltage can increase operating temperature, requiring effective heat dissipation. Combining with the heat increase assessment to choose, combined with further evaluation of heat dissipation methods is needed. To balance these factors, based on simulation results, V_{GS} can be selected in the range of -2.4 V ÷ -2 V.

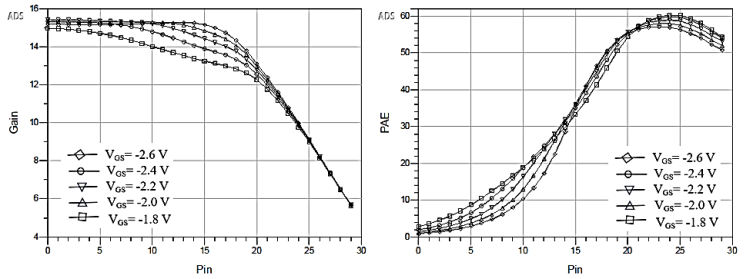


Figure 11. *Performance of the circuit when changing V_{GS}.*

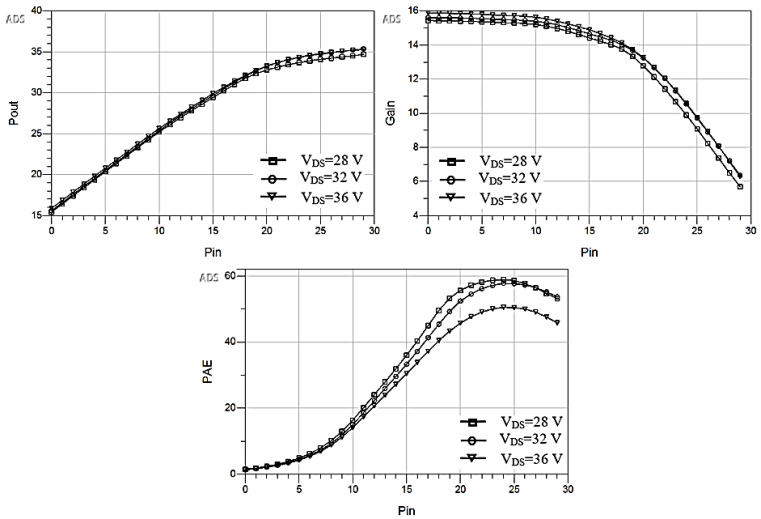


Figure 12. *Performance of the circuit when changing V_{DS}.*

To continue selecting the bias voltage V_{DS}, perform a simulation with V_{GS} = -2.4 V, evaluate the output power, Gain and PAE when changing the received VDS as shown in figure 12. V_{DS} increases gradually for increasing P_{out}, Gain increases when P_{in} is low, then decreases due to power compression, PAE decreases gradually. V_{DS} = 36 V, PAE decreases significantly at $P_{in} \geq 20$ dBm, posing a major heat dissipation problem. To balance between the criteria, choose $V_{DS} = (28 \div 32)$ V.

The results of the investigation of the influence of transistor size and bias voltage on circuit performance are summarized in table 2.

Table 2. *Summary of the effects of size and bias voltage on circuit performance.*

Configuration (size / bias)	**Stability (K, MAG, f_{max})**	**P_{out} & Gain**	**PAE**	**Remarks/Other effects**
2×75 µm	K < 1 in Ku-band, prone to oscillation; high MAG, large f_{max}	Low Pout, moderate Gain	Low PAE	Minor trapping; suitable only for driver stage
2×125 µm	More stable than 2×75 but still requires RC/stub network	Higher Pout than 2×75	Slightly improved PAE	Easier matching (Z closer to Smith center)
4×125 µm	K < 1 in Ku-band; f_{max} reduced compared to 2×125	Good P_{out} and Gain; fairly linear	Balanced PAE	Trapping effects are noticeable; suitable for the driver stage
6×125 µm	K ≈ 1 @14 GHz, small stability margin	Higher Pout and Gain than 4×125	Good PAE at $P_{in} \geq 24$ dBm	Requires careful control of trapping & heating
6×150 µm	K > 1 in Ku-band; improved stability	Pout not higher than 6×125	Lower PAE due to large P_{DC}	Increased parasitics, more difficult matching
8×125 µm	K dips at 18÷25 GHz, risk of out-of-band oscillation	Pout comparable to 6×125 at high Pin	Poor PAE	Strong trapping & thermal effects, challenging matching
VGS	↑ *VGS* →↑ *stability*	Better linearity at higher VGS	PAE decreases due to higher P_{DC}	Recommended V_{GS} = –2.4 ÷ –2 V for balance
VDS	↑ *VDS* →↑ *stability*	Larger P_{out} but PAE drops significantly at V_{DS} > 32 V	Heating & reliability concerns	Recommended VDS = 28 ÷ 32 V

5. CONCLUSIONS

The paper has presented the method of performing simulations, the way of analyzing simulation results, and commented on the effects of choosing transistor size, bias voltage affecting small signal parameters such as stability, maximum power amplification factor (MAG) and large signal parameters Pout, Gain, PAE of an MMIC PA. As well as taking into account the required impedance matching circuit factor affecting the loss due to impedance matching, circuit size, and cost, from which to make the optimal choice of tube size and bias voltage. From table 2, it can be seen that a too small size (2x125, 4x125) is less stable, increasing the size to better stability (6x125, 6x150), but too large (8x125) is less stable, and easy to oscillate out of range. Increasing the size can increase the saturation power, increase gain, and PAE in the large input signal level region.

Depending on the position of the amplifier stage, there are input levels and priority requirements for gain or Pout, so there are appropriate size options. In addition, when the size increases, it leads to more complex impedance matching, increased loss, reduced bandwidth, and increased circuit size. In addition, increasing the size leads to increased trapping effects, leakage current, parasitic and local heat problems, so when the size is large, P_{out} does not increase proportionally with the increase in size, and PAE may be reduced. Therefore, choosing the size of the transistor needs to trade off all these factors and usually choose a smaller size (4×125 or 2×125) for the driver stage and a larger size (6×125 or 6×150) for the final amplifier stage.

With the bias problem, increasing the bias voltage will increase P_{out}, increasing Gain not much, but will significantly reduce PAE because the increased output power cannot compensate for the amount of static power and leads to the problem of self-heating, requiring effective heat dissipation measures. Therefore, it is necessary to choose a balance operating point between these factors, V_{GS} about -2.4 V to -2.0 V, V_{DS} about 28 V÷32 V to balance Pout, Gain, PAE and limit heat.

During the simulation execution process, these analysis steps can be applied to analyze and select in other MMIC PA designs. The next research direction of the author group is to study how to optimize transistor size for a wideband power amplifier.

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TÓM TẮT

Tối ưu hóa kích thước và điện áp thiên áp nâng cao hiệu năng bộ khuếch đại MMIC công suất cao sử dụng công nghệ GaN

Bài báo trình bày phương pháp tối ưu hóa điện áp thiên áp và kích thước bóng bán dẫn nhằm nâng cao hiệu suất chuyển đổi công suất (PAE) và công suất đầu ra trong bộ khuếch đại công suất cao sử dụng công nghệ GaN MMIC. Sử dụng mô phỏng với bóng bán dẫn MP2500S trên nền tảng công nghệ WIN NP25 trong phần mềm ADS, nhóm nghiên cứu đã tiến hành phân tích ảnh hưởng của các mức điện áp VGS, VDS và kích thước cực cổng khác nhau đến các chỉ tiêu PAE, công suất đầu ra và hệ số khuếch đại. Các kết quả mô phỏng và phân tích được áp dụng cho bộ khuếch đại đường lên thông tin vệ tinh (14 ÷ 14.5 GHz) với các cấu hình độ rộng cổng từ 2 x 75 µm đến 8 x 125 µm. Các kết quả chỉ ra rằng, với độ rộng cổng phù hợp, sự lựa chọn điểm làm việc ở chế độ AD có thể cải thiện đáng kể hiệu năng PAE trong khi vẫn đảm bảo công suất ra Pout. Tuy nhiên, nghiên cứu cũng chỉ ra rằng khi kích thước cổng quá lớn có thể làm giảm hiệu năng mạch do hiệu ứng bẫy, các dòng dò kí sinh và hiệu ứng tự làm nóng. Bài báo đề xuất một phương pháp phân tích lựa chọn kích thước bóng bán dẫn và điểm thiên áp tối ưu trong thiết kế GaN PA, đặc biệt là các ứng dụng yêu cầu công suất lớn và hiệu suất cao trong băng tần Ku (12 ÷ 18 GHz). Nghiên cứu này đóng góp vào việc nâng cao hiệu năng của GaN HEMT trong các ứng dụng điện tử công suất.

Keywords: GaN HEMT; Độ rộng cổng; Điện áp thiên áp; Khuếch đại công suất; Băng Ku; WIN NP25; Load-pull.