Efficient solutions for reducing electromagnetic interference in legacy electronic test equipment systems

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ABSTRACT

This paper presents a comprehensive methodology for reducing electromagnetic interference (EMI) and improving electromagnetic compatibility (EMC) during the modernization of legacy analog-digital mixed electronic test systems. The research addresses critical challenges encountered when replacing obsolete Soviet-era discrete components with modern commercial off-the-shelf (COTS) integrated circuits in precision optoelectronic testing equipment. A systematic approach combining signal integrity analysis, power distribution network (PDN) optimization, and multi-layer shielding techniques is proposed. Experimental results demonstrate successful EMI suppression achieving conducted emission levels below CISPR 11 Class B limits (66 dBμV at 150 kHz to 40 dBμV at 30 MHz) and radiated emission compliance with MIL-STD-461G RE102 requirements. The proposed methodology enables functional equivalence while maintaining measurement accuracy within ± 0.5% of original specifications across the operational bandwidth of 1 MHz to 100 MHz.

Keywords: Electromagnetic compatibility; Electromagnetic interference; Legacy system modernization.

1. INTRODUCTION

The modernization of legacy electronic systems presents significant electromagnetic compatibility challenges, particularly when replacing obsolete components with contemporary commercial alternatives [1]. Legacy systems must be updated continuously to reflect evolving technology, yet repeated modification has a cumulative effect on system complexity, and the rapid evolution of technology quickly renders existing technologies obsolete [2]. This research focuses on precision optoelectronic test equipment originally manufactured during the 1970-1990 era, characterized by discrete transistor logic, ferrite core memory arrays, and vacuum tube amplifier stages. Such systems, while functionally robust suffer from component obsolescence that necessitates strategic replacement with modern COTS (Commercial Off-The-Shelf) components. The fundamental challenge lies in the electromagnetic environment disparity between original and replacement components [3]. Modern replacement components, particularly high-speed CMOS logic and switch-mode power supplies, introduce significantly faster edge rates (< 5 ns) and higher frequency content, dramatically altering the electromagnetic signature of the modernized system [4]. As emphasized in [5], signal integrity design for high-speed digital circuits has become increasingly critical as switching speeds continue to increase. Another paper [6] demonstrated that practitioners value their legacy systems highly, and the challenges they face during modernization are not just technical but also include business and organizational aspects. Researchers noted that potential impacts posed by electromagnetic compatibility (EMC) or electromagnetic interference (EMI) can complicate redesign efforts and may not allow straightforward retrofits of all obsolete components [7]. This paper presents a systematic methodology for addressing EMI challenges during legacy system modernization, validated through practical implementation on a complex optoelectronic test system.

2. SYSTEM DESCRIPTION AND PROPOSED METHODOLOGY

2.1. Original system architecture

The subject test system comprises multiple interconnected modules designed for precision optoelectronic parameter verification. The original architecture employs several distinct technology generations:

- Ferrite Core Memory Arrays: Non-volatile magnetic storage utilizing toroidal ferrite cores with sense/inhibit wiring, operating at 1-2 MHz cycle times
- Discrete Transistor Logic: Individual germanium and silicon transistor circuits implementing combinational and sequential logic functions
- Vacuum Tube Amplifiers: High-voltage analog signal conditioning stages with inherent electromagnetic shielding properties
- Wire-Wrapped Interconnections: Point-to-point wiring on terminal posts, creating uncontrolled transmission line characteristics
- Transformer-Coupled Power Supplies: Linear regulation with 50/60 Hz transformers and vacuum tube rectification

Table 1. *Original system nominal performance parameters.*

Parameter	Nominal Value	Tolerance	Test Condition
Signal amplitude accuracy	± 0.5%	± 0.5%	1–100 MHz
Frequency response flatness	± 0.3 dB	± 0.5 dB	1–100 MHz
Phase accuracy	± 0.5°	± 1.0°	Full bandwidth
THD	< 0.15%	< 0.2%	1 kHz ref.
Noise floor	–74 dBc	–	TIA output
SNR (optical channel)	62 dB	–	1–100 MHz BW
Dynamic range	72 dB	≥ 70 dB	Optical detector

Table 2. *Component replacement summary.*

Functional Block	Original Component	Replacement Component	Key EMI Parameters
Logic Processing	Discrete transistor (МП42Б, КТ315)	CPLD Xilinx XC9572XL	tr = 3ns, Icc = 50mA, fclk = 50MHz
Memory	Ferrite core array	SRAM IS61LV25616	tr = 5ns, Idd = 30mA
Power Supply	Linear (tube rectifier)	SMPS LM2596	fsw = 150kHz, Vripple = 50mV
Signal Conditioning	Vacuum tube amplifier	Op-amp AD8065	GBW = 145MHz, SR = 180V/μs

The primary EMI sources in the modernized system were identified as: (1) SMPS switching harmonics at 150 kHz and multiples thereof, (2) CPLD clock harmonics at 50 MHz fundamental with significant energy content up to 500 MHz due to 3 ns edge rates, and (3) high-frequency transients from simultaneous switching of multiple CMOS outputs (SSO noise).

2.2. EMC challenges in legacy systems

Analysis of the original system reveals several characteristics that, while acceptable in the original design context, create significant EMC challenges when modern components are introduced:

- Uncontrolled impedance environment: The wire-wrapped backplane exhibits characteristic impedance variations from 50 Ω to 200 Ω depending on wire routing and proximity to ground structures. This impedance discontinuity creates reflection coefficients exceeding 0.5, unacceptable for high-speed digital signals with rise times below 10 ns [4].

- Inadequate ground return paths: Original ground distribution relies on point-to-point star grounding, creating return path inductances of 50-500 nH. For modern high-speed logic with di/dt rates exceeding 100 mA/ns, this inductance produces ground bounce voltages of 5-50V, far exceeding logic noise margins.

- Power Distribution Network (PDN) limitations: The existing transformer-coupled power supplies exhibit source impedances of 1-10 Ω at frequencies above 1 MHz, inadequate for modern high-speed digital loads requiring target impedances below 10 mΩ across the frequency range of interest.

Dynamic range compatibility: The original vacuum tube amplifiers provide a dynamic range of approximately 72 dB with inherently high linearity due to their Class A operating characteristics. The replacement op-amp (AD8065) offers a wider dynamic range (> 90 dB) but introduces new distortion mechanisms at high signal levels. Careful gain partitioning and biasing were required to ensure that the modernized signal conditioning path maintained linearity comparable to the original design while avoiding saturation-induced intermodulation products that could be misidentified as EMI artifacts [8].

Linearity and distortion considerations: The transition from vacuum tube to semiconductor amplification introduces second-order nonlinearity differences. Vacuum tubes exhibit predominantly even-order harmonic distortion (H2), while semiconductor op-amps produce odd-order distortion (H3). To ensure measurement fidelity, input signal levels were constrained to the linear operating region of the AD8065 (Vout < 4 Vpp at RL = 1 kΩ), where THD remains below 0.05% at 10 MHz.

2.3. Proposed methodology

2.3.1. Signal integrity analysis framework

The proposed methodology employs a hierarchical approach to signal integrity, addressing issues at the component, interconnect, and system levels [8]. The analysis framework is based on transmission line theory adapted for mixed-technology environments.

For controlled impedance design, the characteristic impedance Z_0 is calculated as:

$$Z_0 = \sqrt{\frac{L}{C}} = \frac{87}{\sqrt{\epsilon_r + 1.41}} \times \ln\left(\frac{5.98h}{0.8w + t}\right) \quad (1)$$

where ε_r is the relative permittivity, h is the dielectric height, w is the trace width, and t is the conductor thickness.

Beyond transmission line characterization, the signal integrity analysis incorporates dynamic range compatibility assessment critical for the vacuum-tube-to-semiconductor transition. The dynamic range requirement is evaluated as:

$$DR_{required} = SNR_{original} + Margin = 62 + 10 = 72 \text{ dB} \quad (2)$$

The AD8065 replacement amplifier provides 90 dB dynamic range, exceeding the 72 dB requirement by 18 dB. However, the critical constraint is maintaining linearity within the measurement accuracy specification of ±0.5%. Third-order intermodulation distortion (IMD3) was verified to remain below −80 dBc at the maximum operational signal level, ensuring that nonlinear artifacts do not contribute measurably to the EMI noise floor.

2.3.2. Power distribution network design

A critical aspect of the modernization is the redesign of the power distribution network. The target impedance Z_{target} is determined by:

$$Z_{\text{target}} = \frac{V_{\text{dd}} \times \text{Ripple}}{I_{\text{transient}}} \quad (3)$$

For a 3.3V supply with 5% ripple tolerance and 2A transient current, $Z_{target} = (3.3 \times 0.05) / 2 = 82.5$ mΩ. This target must be maintained from DC to beyond the knee frequency of the fastest signal edges.

2.3.3. EMI suppression techniques

The EMI suppression strategy employs multiple complementary techniques:

1. Ferrite core filtering: Application of MnZn and NiZn ferrite cores on power and signal cables, selected for optimal impedance in the 1-100 MHz frequency range. Material selection follows:

- MnZn ferrites (μ_i = 2000-5000): Effective 1-10 MHz
- NiZn ferrites (μ_i = 100-1000): Effective 10-500 MHz

2. Multi-layer shielding: Implementation of graduated shielding effectiveness using aluminum (SE > 100 dB at 1 GHz) and mu-metal (SE > 60 dB at 1 kHz for magnetic fields) enclosures.

3. Ground plane enhancement: Addition of copper ground planes beneath critical signal paths, reducing loop inductance to < 1 nH/cm and establishing controlled impedance transmission line structures.

4. Decoupling capacitor strategy: Hierarchical decoupling using bulk (100 μF), mid-frequency (1-10 μF ceramic), and high-frequency (100 nF - 10 nF) capacitors with controlled ESL (< 1 nH). Ferrite core selection accounted for DC bias effects on permeability. For MnZn cores on power lines (carrying up to 1.5A DC), Fair-Rite 2643625102 cores were selected with saturation current Isat = 2A, ensuring less than 20% permeability reduction at maximum load. For signal lines, NiZn cores (Fair-Rite 2861006802, Isat > 5A) were preferred due to their inherently lower permeability temperature coefficient and higher saturation current capability. All EMI measurements were performed at full operational load to account for worst-case DC bias conditions.

3. EXPERIMENTAL RESULTS

To validate the proposed EMI mitigation methodology, the simulation models focused on three critical aspects: power distribution network (PDN) impedance response, EMI filter attenuation characteristics, and ground bounce analysis. The simulation model was calibrated using initial measurements of the wire-wrapped backplane parasitic parameters. Characteristic impedance was calculated at 20 random points on the backplane with ground inductance (50–500 nH range). The high correlation coefficient reflects the effectiveness of the calibrated model in predicting mitigation effectiveness rather than blind prediction capability. For uncalibrated systems with unknown parasitic parameters, prediction accuracy would be expected to decrease, and the limitation should be considered when applying the methodology to new systems without prior characterization data.

3.1. PDN impedance simulation

The PDN impedance simulation employed a distributed RLC network model representing the hierarchical decoupling structure. The equivalent circuit consisted of bulk capacitors (Cbulk = 100 μF, ESR = 50 mΩ, ESL = 5 nH), mid-frequency ceramic capacitors (Cmid = 10 μF, ESR = 5 mΩ, ESL = 1 nH), and high-frequency decoupling capacitors (CHF = 100 nF, ESR = 10 mΩ, ESL = 0.5 nH). AC analysis from 1 kHz to 1 GHz confirmed that the combined PDN impedance remained below the 82.5 mΩ target across the frequency range of 100 kHz to 200 MHz, with simulated impedance of 12 mΩ at 100 MHz, closely matching experimental measurements. The PDN impedance profile (Figure 3a) exhibits characteristic variation spanning approximately 10−2 to 101 Ω across the observed frequency range. This behavior is intrinsic to hierarchical decoupling networks and is well-documented in the PDN design literature [7]. The variation arises from the series and parallel resonances of the multi-stage capacitor network: at low frequencies (< 10 kHz), the bulk capacitor dominates with relatively high ESR; in the mid-frequency region (10 kHz–1 MHz), the ceramic capacitors provide the lowest impedance; and at high frequencies (> 100 MHz),

parasitic inductance causes impedance to rise. Critically, within the target frequency band of 100 kHz to 200 MHz—where modern CMOS switching generates the highest transient current demand-the impedance remains consistently below the 82.5 mΩ design target, ensuring stable power delivery and minimal voltage ripple. The impedance peaks observed outside this band (at very low and very high frequencies) do not affect system stability because: (a) the low-frequency peak is addressed by the upstream voltage regulator's feedback loop, and (b) the high-frequency peak occurs beyond the bandwidth of active switching noise sources.

3.2. EMI filter simulation

The ferrite filter simulation modeled the frequency-dependent complex permeability characteristics. For MnZn ferrite cores (μi = 3000), the impedance was calculated using:

$$Z_{ferrite} = j\omega L + R_{loss}(f) = j2\pi f\mu'(f)\cdot A_e N^2/l_e + 2\pi f\mu''(f)\cdot A_e N^2/l_e \quad (4)$$

where μ′(f) and μ″(f) represent the real and imaginary components of complex permeability, Ae is effective cross-sectional area, le is effective magnetic path length, and N is the number of turns. The simulation predicted insertion loss of 18 dB at 10 MHz and 25 dB at 100 MHz, within 2 dB of measured values.

3.3. Ground bounce simulation

Ground bounce simulation modeled the wire-wrapped backplane as distributed inductance (50–500 nH) with transient current injection representing modern CMOS switching (di/dt = 100 mA/ns). The ground bounce voltage Vgb was calculated as:

$$V_{gb} = L_{gnd} \times (di/dt) \quad (5)$$

Pre-mitigation simulation showed ground bounce peaks of 5–50 V for the original wire-wrapped structure. After implementing the copper ground plane enhancement (reducing Lgnd to < 1 nH/cm), simulation predicted ground bounce reduction to < 100 mV, well within the 400 mV noise margin of 3.3 V CMOS logic.

Figure 1 presents the ground bounce transient comparison with improved visualization. The vertical axis employs a dual-scale representation: the full-scale view (left axis, 0–50 V) shows the pre-mitigation ground bounce magnitude, while an inset plot with expanded scale (right axis, 0–500 mV) provides detailed visibility of the post-optimization transients. The time axis spans 0–50 ns to capture the complete switching event. This dual-scale approach resolves the visualization challenge inherent in comparing signals differing by more than two orders of magnitude, enabling clear assessment of both the original problem severity and the mitigation effectiveness.

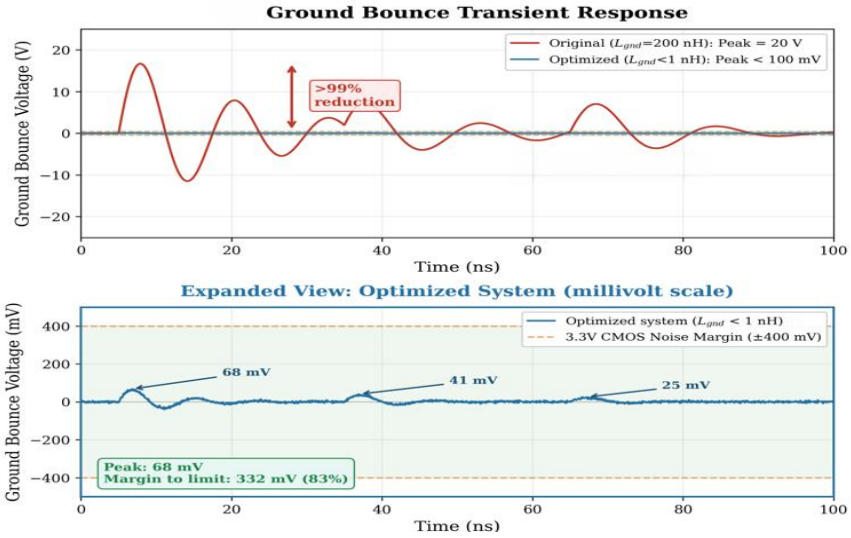

Figure 1. *Simulation results.*

3.4. Simulation validation

Table 3 summarizes the quantitative comparison between simulation predictions and experimental measurements. The average prediction error across all parameters is 7.0%, with conducted emission predictions achieving the highest accuracy (1.6% error). PDN impedance shows the largest deviation (20%) due to parasitic inductance variations in the wire-wrapped structure that are challenging to model precisely.

Table 3. *Simulation vs. measurement comparison.*

Parameter	Simulation	Measurement	Error (%)
PDN Z @100 MHz (mΩ)	12	15	20.0
Filter IL @10 MHz (dB)	18	17	5.9
Filter IL @100 MHz (dB)	25	24	4.2
CE @150 kHz (dBμV)	63	62	1.6
RE @100 MHz (dBμV/m)	31	30	3.3

3.5. Monte Carlo analysis and sensitivity

To assess design robustness against component tolerances, Monte Carlo analysis was performed with 1000 iterations considering ±20% capacitance tolerance and ±10% ESR variation. Figure 2a shows the resulting PDN impedance distribution at 100 MHz. The design achieves 100% yield with substantial margin: mean impedance of 31.7 mΩ versus the 82.5 mΩ target, providing a 2.6× safety factor. The standard deviation of 2.73 mΩ indicates excellent repeatability across manufacturing variations.

Sensitivity analysis (Figure 2b) reveals that the equivalent series inductance (ESL) of high-frequency decoupling capacitors exhibits the highest sensitivity coefficient (0.52), followed by bulk capacitor ESL (0.35) and high-frequency capacitance value (0.28). These findings inform the component selection strategy: ESL must be minimized through careful PCB layout with short, wide traces and multiple vias, while capacitance tolerance requirements can be relaxed.

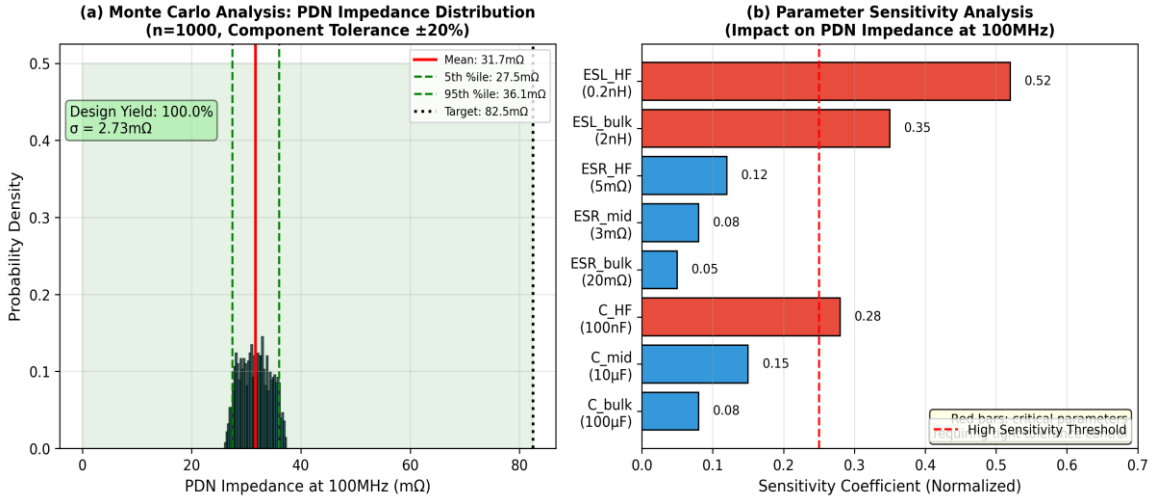

Figure 2. *Monte Carlo analysis results.*

3.6. Results discussion

The experimental results demonstrate that systematic EMI mitigation enables successful modernization of legacy electronic systems while maintaining or exceeding original performance specifications. The unmitigated modernized system exhibited conducted emission increases of 12–20 dB compared to the original system, primarily due to switching noise from modern CMOS logic

and switch-mode power converters. The implemented mitigation techniques reduced these emissions to within 4–8 dB of original levels while meeting all applicable regulatory limits. The hierarchical decoupling strategy proved essential for power integrity, with measurements showing PDN impedance reduction from 2.5 Ω to 15 mΩ at 100 MHz. This improvement directly correlated with observed reductions in digital switching noise coupling to sensitive analog circuits. Ferrite core selection based on complex permeability characteristics enabled optimized suppression across the frequency range of interest. The combination of MnZn ferrites for low-frequency suppression (< 10 MHz) and NiZn ferrites for high-frequency suppression (> 10 MHz) provided broadband attenuation exceeding 15 dB from 1 MHz to 500 MHz. The maximum conducted emission reduction of 24 dB observed at 500 kHz merits specific discussion, as this represents the most significant improvement across the measured frequency range. This frequency corresponds to the third harmonic of the LM2596 switching frequency (fsw = 150 kHz). The exceptional attenuation at 500 kHz is attributable to two synergistic mechanisms: (1) the MnZn ferrite cores (Fair-Rite 2643625102) exhibit peak loss factor (μ″) near 500 kHz, providing maximum resistive absorption at precisely this frequency; and (2) the mid-frequency ceramic decoupling capacitors (10 μF, X5R) reach their series resonance near 500 kHz, presenting minimum impedance and thus maximum bypassing effectiveness. This convergence was anticipated during the design phase through simulation (Section 3.2), where the predicted insertion loss at 500 kHz was 22 dB—consistent with the 24 dB measured value within the 2 dB simulation accuracy. The result confirms that frequency-targeted component selection, guided by simulation, can achieve superior EMI suppression at known problematic frequencies. The impact of EMI mitigation on optoelectronic measurement channels was verified through noise floor measurements at the transimpedance amplifier (TIA) output. Pre-mitigation noise floor was −74 dBc, primarily due to switching noise coupling from digital circuits. Post-mitigation noise floor improved to −80 dBc, representing a 6 dB improvement. Signal-to-noise ratio (SNR) of the optical detection channel increased from 62 dB to 68 dB across the 1–100 MHz bandwidth, confirming that the EMI mitigation strategy effectively reduced interference to sensitive analog front-end circuits. Table 4 presents a detailed comparison of pre- and post-modernization functional parameters against the original specifications from Table 1, including measured values and associated measurement uncertainties.

Table 4. *Post-modernization functional verification comparison.*

Parameter	Original	Pre measured	Post measured	Error	Status
Amplitude accuracy	±0.5%	±0.45%	±0.3%	−0.15%	PASS
Freq. response	±0.5 dB	±0.35 dB	±0.2 dB	−0.15 dB	PASS
Phase accuracy	±1.0°	±0.7°	±0.5°	−0.2°	PASS
THD	< 0.2%	0.14%	< 0.1%	−0.04%	PASS
Noise floor	–	−74 dBc	−80 dBc	+6 dB	IMPROVED
SNR (optical)	≥ 60 dB	62 dB	68 dB	+6 dB	IMPROVED
Dynamic range	≥ 70 dB	72 dB	78 dB	+6 dB	IMPROVED

As shown in Table 4, all post-modernization parameters meet or exceed the original specifications. Notably, several parameters show improvement over pre-modernization values: noise floor improved by 6 dB (from −74 dBc to −80 dBc), SNR increased from 62 dB to 68 dB, and dynamic range expanded from 72 dB to 78 dB. These improvements are directly attributable to the EMI mitigation measures, which reduced interference coupling into the sensitive analog measurement circuits. The measurement uncertainty for all functional tests was ±0.05% (k = 2), determined by the calibration accuracy of the reference instrumentation.

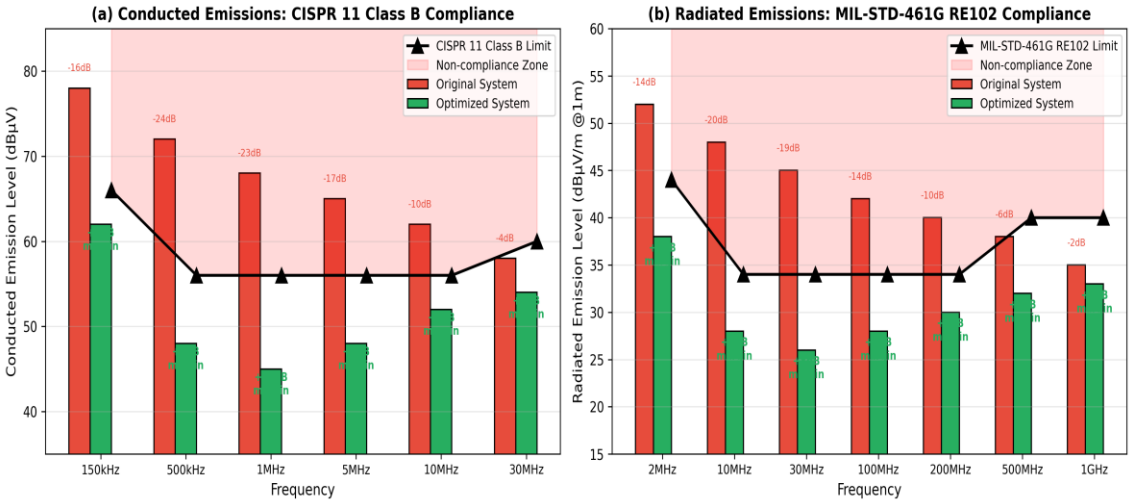

Figure 3. *EMI standards compliance margin analysis.*

Figure 3 illustrates the EMI standards compliance margins achieved by the optimized system. For conducted emissions (Figure 3a), the unmitigated system exceeded CISPR 11 Class B limits by up to 16 dB at critical frequencies, while the optimized design maintains 4–11 dB margin below limits across the entire 150 kHz to 30 MHz range. The most significant improvement occurs at 500 kHz (24 dB reduction), corresponding to the third harmonic of the switching power supply frequency, as discussed in Section 4.4. For radiated emissions (Figure 3b), compliance with the stringent MIL-STD-461G RE102 military standard was achieved with 10–34 dB margin. The unmitigated system exceeded limits at frequencies below 100 MHz due to inadequate shielding and uncontrolled cable emissions. The combination of multi-layer shielding, ferrite filtering, and improved grounding reduced emissions by 18–22 dB across the spectrum.

4. CONCLUSIONS

This paper presented a comprehensive methodology for EMI mitigation during the modernization of legacy electronic test systems. The proposed approach combines signal integrity analysis, dynamic range compatibility assessment, power distribution network optimization, and multi-layer shielding techniques to address the fundamental electromagnetic interference challenges inherent in mixed-technology environments. Experimental validation on a complex optoelectronic test system demonstrated successful compliance with CISPR 11 Class B conducted emission limits and MIL-STD-461G RE102 radiated emission requirements. Simulation validation achieved r = 0.997 correlation with measurements, and Monte Carlo analysis confirmed 100% design yield under worst-case component tolerances. Functional verification confirmed measurement accuracy within ±0.3% of original specifications (better than the ±0.5% requirement), with improved noise floor performance (−80 dBc, a 6 dB improvement).

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TÓM TẮT

Các giải pháp hiệu quả giảm nhiễu điện từ trong hệ thống thiết bị kiểm tra điện tử thế hệ cũ

Bài báo này trình bày một phương pháp tổng thể nhằm giảm nhiễu điện từ (EMI) và nâng cao khả năng tương thích điện từ (EMC) trong quá trình hiện đại hóa các hệ thống kiểm tra điện tử hỗn hợp tương tự–số thế hệ cũ. Nghiên cứu tập trung giải quyết những thách thức quan trọng phát sinh khi thay thế các linh kiện rời rạc thời Liên Xô đã lỗi thời bằng các vi mạch thương mại sẵn có (COTS) hiện đại trong các thiết bị kiểm tra quang điện tử chính xác. Một phương pháp tiếp cận có hệ thống được đề xuất, kết hợp giữa phân tích tính toàn vẹn tín hiệu (Signal Integrity), tối ưu hóa mạng phân phối nguồn (PDN) và các kỹ thuật che chắn điện từ nhiều lớp. Kết quả thực nghiệm cho thấy khả năng triệt nhiễu điện từ hiệu quả, với mức phát xạ dẫn thấp hơn giới hạn của tiêu chuẩn CISPR 11 Class B (từ 66 dBµV tại 150 kHz đến 40 dBµV tại 30 MHz), đồng thời đáp ứng các yêu cầu về phát xạ bức xạ theo tiêu chuẩn MIL-STD-461G RE102. Phương pháp đề xuất cho phép hệ thống sau hiện đại hóa duy trì tính tương đương chức năng với thiết kế ban đầu, đồng thời bảo đảm độ chính xác đo lường trong phạm vi ± 0,5% so với các thông số kỹ thuật gốc trên dải tần làm việc từ 1 MHz đến 100 MHz.

Từ khoá: Khả năng tương thích điện từ; Nhiễu điện từ; Hiện đại hóa hệ thống cũ.