A reliable centralized real-time multi-protocol data collection module for mission-critical vessel systems

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ABSTRACT

Sensor networks deployed on modern vessels operate under heterogeneous communication protocols and stringent real-time constraints, necessitating a mission-critical, centralized solution for deterministic data acquisition and pre-processing. This paper presents the design and implementation of an FPGA-based sensor data collection and reconstruction module that supports the simultaneous integration of MIL-STD-1553B, ARINC-429, and RS-422/485 interfaces within a unified architecture. System reliability and fault tolerance are enhanced through support for error-correction coding and the use of high-bandwidth on-chip memory in place of conventional off-chip storage, ensuring deterministic performance for real-time operation. Following acquisition and normalization, sensor data are aggregated and transmitted to a central monitoring system via a high-speed Ethernet interface. Experimental validation demonstrates stable operation, improved data integrity, and compliance with real-time processing requirements in complex environments.

Keywords: FPGA; MIL-STD-1553B; Block RAM; Hamming code; Ethernet; ARINC-429.

1. INTRODUCTION

Modern mission-critical vessel systems integrate heterogeneous subsystems operating under multiple communication standards such as MIL-STD-1553B, ARINC-429, and RS-422/485 [1-3]. While each protocol ensures reliable communication for its specific application domain—particularly MIL-STD-1553B with its deterministic command/response mechanism [1, 4]—their coexistence within a single platform introduces significant challenges in data aggregation and real-time synchronization.

In conventional architectures, each communication interface is processed separately and later merged at higher software layers. This distributed approach increases system complexity, adds latency, and complicates deterministic timing control, which is critical in mission-oriented naval environments [4, 5].

To address these limitations, a centralized hardware-based architecture capable of simultaneously acquiring and processing multi-protocol data streams is required. By integrating MIL-STD-1553B, ARINC-429, and RS-422/485 interfaces into a single FPGA platform, heterogeneous data frames can be received in parallel, validated, normalized into a unified internal format, and aggregated deterministically. The standardized data are then transmitted to a central monitoring system via a high-speed Ethernet interface, simplifying upper-layer processing and improving overall system efficiency and robustness.

The main contributions of this paper are summarized as follows:

1) *A unified hardware architecture* that enables the simultaneous reception, aggregation, and standardization of data streams from MIL-STD-1553B, ARINC-429, and RS-422 interfaces within a single FPGA-based system.

2) An enhanced MIL-STD-1553B communication module incorporating an extended Hamming code–based error-correction scheme to provide automatic single-bit error correction, thereby overcoming the limitations of the conventional parity-only mechanism. In addition, external memory is replaced with on-chip block RAM (BRAM), improving bandwidth, reducing latency, and enhancing system robustness [7, 8].

The remainder of this paper is organized as follows. Section 2 presents the theoretical foundations of multi-protocol integration and error-correction mechanisms. Section 3 describes the experimental setup and evaluates system performance. Finally, Section 4 concludes the paper.

2. PROBLEM AND SOLUTION

2.1. MIL-STD-1553B standard processing

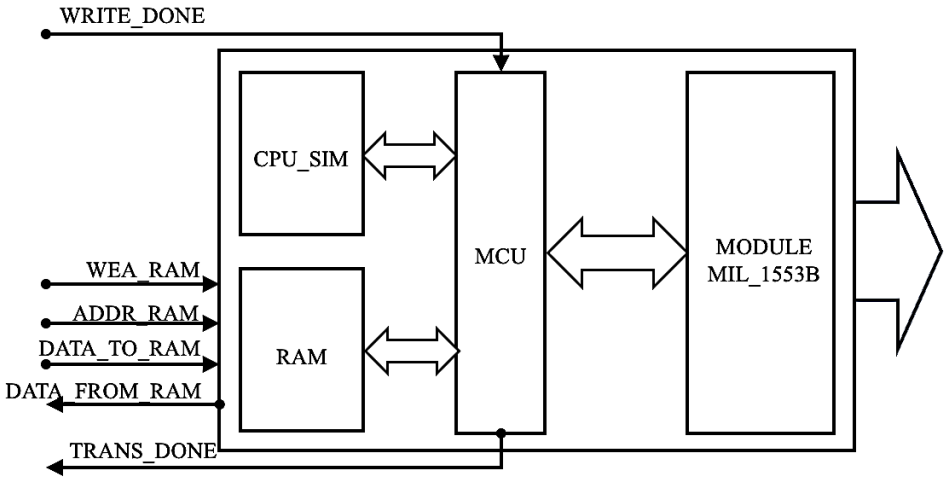


Figure 1. *MIL-STD-1553B block design diagram.*

Figure 1 illustrates the proposed MIL-STD-1553B processing architecture integrated within the centralized FPGA-based data acquisition system. Instead of focusing on the protocol specification, the architecture is designed to ensure reliable reception, buffering, aggregation, and forwarding of 1553B data toward the unified data processing pipeline.

The MIL-STD-1553B module performs real-time reception and transmission on the bus and forwards validated data frames to the internal processing subsystem. The MCU block coordinates bidirectional data exchange between the MIL-1553B interface and the internal memory system. Received data words are temporarily stored in on-chip memory (BRAM) through a controlled write mechanism, while status signals such as WRITE_DONE and TRANS_DONE ensure synchronization between acquisition and processing stages.

In practical operation, the data acquisition module must handle not only standard frames but also specific transmission patterns from three function cards: RTx, BC_1, and BC_2, etc, each with distinct BC/RT roles and data formats [1, 4, 5].

The RTx card operates as a x^{th}-remote terminal (RT). The module monitors BC-issued commands addressed to RTx, captures the complete response frame, and extracts up to 32 data words while ensuring packet integrity. The BC_1 card functions as a bus controller (BC) but transmits 47 data words, exceeding the 32-word frame limit of MIL-STD-1553B. Operating at 20 Hz, BC_1 splits the transmission into two consecutive sessions (CMD1: 32 words, CMD2: 15 words). The system must detect and associate these command pairs, merge the two sessions into a single 47-word packet in BRAM, and then forward it for Ethernet aggregation. The BC_2 card also operates as a BC, periodically broadcasting 12-word packets at 50 Hz. The acquisition module

must synchronize with this cycle, correctly extract each packet from the continuous bit stream, and identify its source to prevent data loss.

All validated data are converted into an internal standardized format and stored in an aggregation buffer shared with other protocol modules. This design allows the MIL-STD-1553B interface to operate as one input channel within a multi-protocol parallel acquisition framework, ensuring deterministic processing and seamless integration with the Ethernet conversion stage described in subsequent sections.

2.2. ARINC-429 standard processing

Figure 2 illustrates the ARINC-429 module integrated into the centralized FPGA-based multi-protocol architecture. In conventional implementations, ARINC-429 interfaces often rely on commercial controller chips that require manual configuration of transmission parameters and software-level frame management [3, 9]. In contrast, the proposed design embeds all protocol processing directly into the FPGA fabric, enabling fully automated operation.

All essential parameters defined by the ARINC-429 standard, including data rate, word formatting, and parity generation [3], are pre-configured in hardware. The TX and RX paths operate as independent parallel threads, while a dual-port RAM provides simultaneous buffering without contention, ensuring deterministic real-time processing.

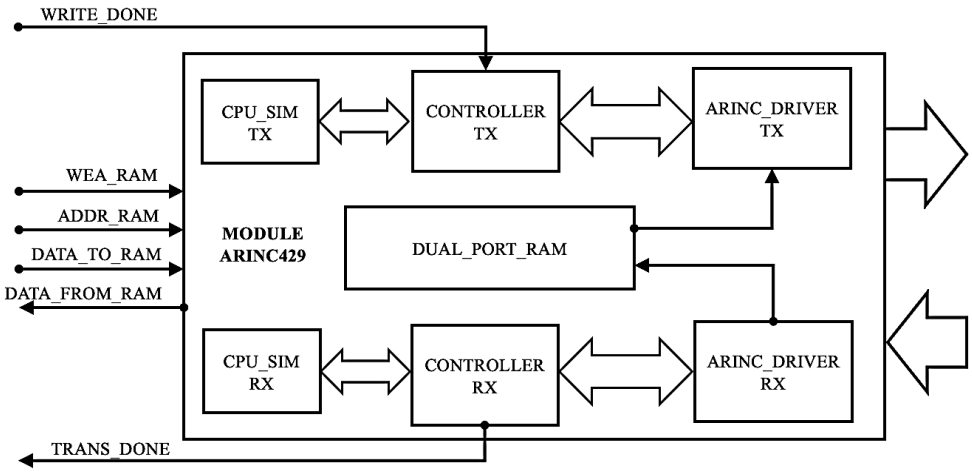


Figure 2. *ARINC-429 block design diagram.*

Incoming bit streams are automatically synchronized, validated, and parsed in hardware, eliminating the need for software intervention. Only verified payload data is forwarded and normalized into a unified internal data structure before being written into the shared aggregation buffer. By integrating configuration, frame handling, and validation entirely in hardware [3, 9], the proposed module reduces processor load and enables seamless integration into the Ethernet-based centralized data conversion architecture.

2.3. RS422/485 standard processing

Unlike fixed-frame standards such as MIL-STD-1553B and ARINC-429, the RS-422 protocol in the system supports asynchronous serial transmission with variable packet lengths. The FPGA module uses a dynamic length determination mechanism based on four end-of-frame control bits to accurately infer the amount of data. When RS-422 data is fed into the cache, the control logic decodes these bits to determine the packet length. This mechanism allows the system to be flexible in both directions of communication without the need to reconfigure the hardware. The data after being separated and normalized will be stored in an intermediate cache, ready for the process of synthesizing multistandard data.

2.4. Integrated extended hamming code algorithm

To overcome the limitations of the traditional odd parity checking mechanism in the MIL-STD-1553B standard, which only detects odd errors and cannot self-correct, the paper proposes a solution. The paper proposes to integrate the extended Hamming code algorithm directly into the physical layer of the FPGA. This solution allows the system to automatically correct single-bit errors and detect double errors, minimizing the need for packet retransmission in a noisy environment. Design principle: The algorithm performs encoding that adds p-check bits to the original data string d (16-bit) based on Hamming [8, 10] inequality (1):

$$2^p \geq p + d + 1 \tag{1}$$

$$n = p + d \tag{2}$$

where d is the number of bits of the original data, p is the number of additional bits, n is the number of bits from the Hamming code calculated according to the formula (2). After receiving the data from the transmitter, decoding is carried out by calculating the syndrome according to the formula (3) as follows [11]:

$$syndrome = \sum_{i=0}^{p} s_i . 2^i \tag{3}$$

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
p0	p1	d0	p3	d1	d2	d3	p7	d4	d5	d6	d7	d8	d9	d10	p15	d11	d12	d13	d14	d15	d16	p22

Figure 3. *MIL-STD-1553B data frame encoding according to extended Hamming coding.*

With 16-bit input data, the system adds 5 bits of Hamming checks and 1 bit of global Parity, which is made up of 23 bits of extension code (Figure 3). The encoding and decoding process is carried out in parallel at the two transmit/receive ends via IP Core blocks. On the encoder side, the encoder block calculates the Hamming bits from the input data and inserts them into the transmission frame before performing the Manchester II encoding to be put on the bus (Figure 4). On the decoder side, the system calculates the Syndrome value from the received data to determine the fault state (Figure 5). Case Syndrome ≠ 0 and the Parity bit reports an error, the system identifies a single-bit error and automatically reverses the bit at the fault location to recover the data in the same processing cycle. Case Syndrome ≠ 0 but the Parity bit is correct. The system identifies double faults and triggers error flags, which require retransmission to be performed to avoid using false data.

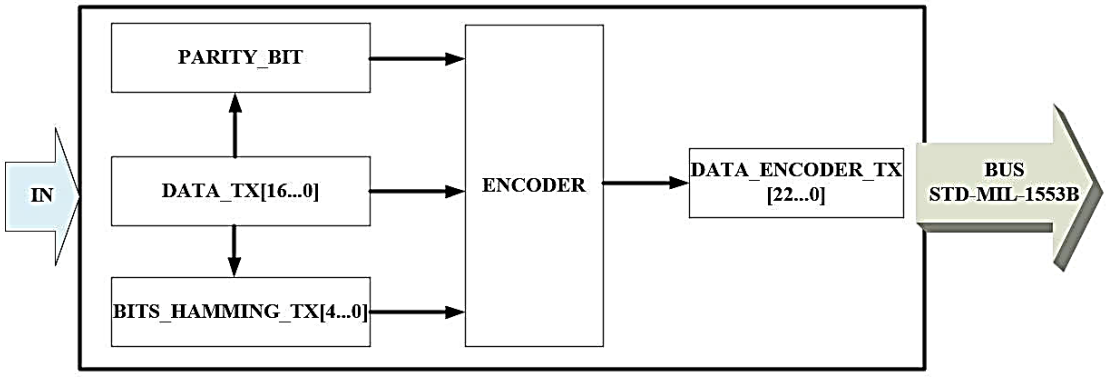


Figure 4. *Built-in Hamming code encoding scheme on TX module.*

This solution ensures higher data integrity than the original design without altering the hardware structure of the wiring on military ships.

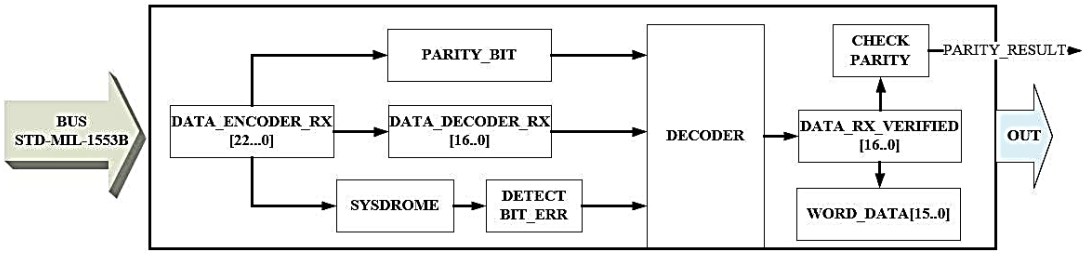


Figure 5. *Hamming code decoding diagram integrated on the RX module.*

2.5. Hardware optimization with on-chip block RAM

Traditional MIL-STD-1553B module designs that use external RAM often face limitations in retrieval latency, bandwidth, and mechanical stability in military environments due to their reliance on I/O communication and discrete components. To overcome these drawbacks, the study proposes to completely replace external RAM with Block RAM (BRAM) built into the Artix-7 FPGA. BRAM is configured as FIFO or Dual-port RAM via IP Core, allowing data retrieval at the system clock and eliminating peripheral communication latency [6, 7].

Figure illustrates the proposed MIL-STD-1553B module architecture, in which the MCU communicates with the module via an interface buffer and address, interrupt, and configuration management blocks. Data from the MCU or MIL-STD-1553B bus is stored in BRAM, processed via an extended Hamming code block, and then encoded/decoded Manchester and transmitted/received on the bus.

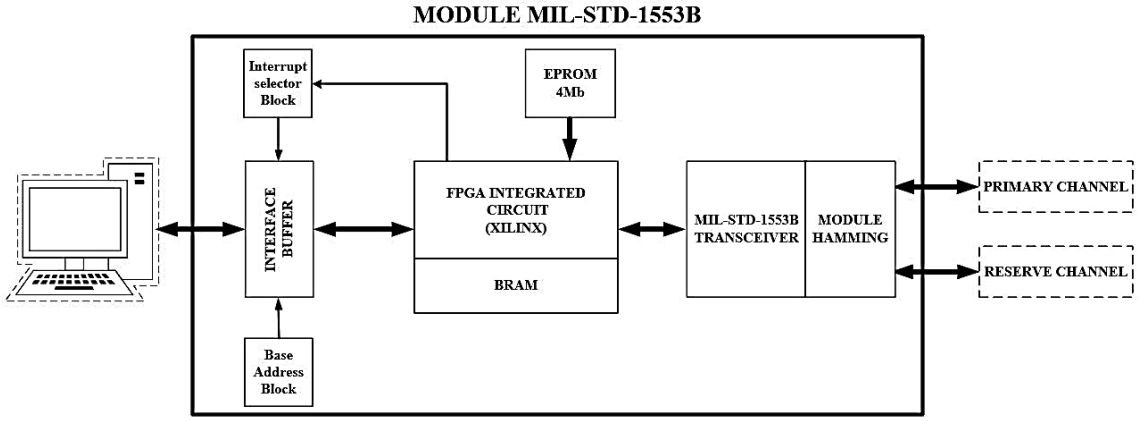


Figure 6. *MIL-STD-1553B diagram using BRAM integrated with an extended Hamming code.*

2.6. Protocol processing and conversion

In the proposed architecture, the Ethernet block acts as a centralized bidirectional gateway between the host computer and the multi-standard communication subsystem. In the upstream direction, data from MIL-STD-1553B, ARINC-429, and RS-422 are acquired in parallel, validated, and buffered. Once complete, sensor data are collected within a processing cycle, the controller organizes and merges individual frames into a unified internal structure, encapsulates them into a standardized Ethernet frame, and transmits them to the host. This ensures synchronized and complete data delivery rather than fragmented protocol-specific packets.

In the downstream direction, Ethernet control frames from the host are decoded and routed to the corresponding protocol module. Each module automatically reconstructs the command into its native format and transmits it to the associated sensor. All frame processing and timing control are implemented in hardware, enabling deterministic and reliable bidirectional communication.

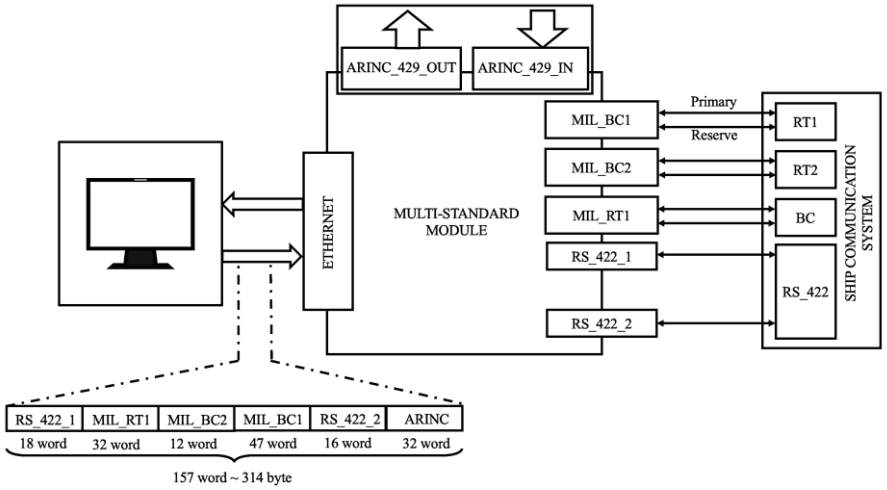


Figure 7. *Diagram of the connection between the simulator module and sensors system.*

Figure 7 illustrates the multi-standard data collection and simulation module in military ship systems, supporting MIL-STD-1553B, ARINC-429 and RS-422 protocols. The module plays the role of an intermediary, receiving and generating data from communication channels, then synthesizing and transmitting via Ethernet according to a unified data structure, effectively serving the monitoring, testing and integration of communication equipment on naval ships.

3. RESULTS AND DISCUSSION

3.1. Evaluation of FPGA resource efficiency

In order to verify the feasibility and effectiveness of the design solution, the entire source code describing the hardware of the MIL-STD-1553B module (including BC, RT function blocks, extended Hamming encoding blocks, and BRAM memory) was compiled and executed on the Artix-7 FPGA platform, XC7A35T chip, using the Vivado 2019.2 tool.

Table 1. *Aggregate system resources on the XC7A35 FPGA.*

Resources	LUT	LUTRAM	FF	BRAM
Usage	899	48	1302	30
Available	20800	9600	41600	50
Utilization rate (%)	4.32	0.50	3.13	60.00

The statistical results of the design's resource consumption after execution are detailed in Table 1. Important parameters include the look-up table (LUT), Flip-Flop (FF), block memory (BRAM), and input/output (IO) buffers. The combined results show that the logical resource usage is very low, with LUTs accounting for 4.32% and Flip-Flops accounting for 3.13%, demonstrating that the architecture of state machines and protocol processing blocks is designed to be efficient, without wasting computational resources. BRAM resources are utilized at 60% (30/50 blocks), reflecting the strategy of completely replacing external RAM with internal memory, allowing for full storage of transmit/receive buffers for both BC and RT modes, while reducing retrieval latency and increasing hardware stability. With more than 95% of the logic resources and 40% of the remaining BRAM, the design is highly scalable for the integration of additional processing cores or advanced algorithms. The experimental results confirm that the integration of the MIL-STD-1553B module with the Hamming error correction mechanism on a single FPGA chip is feasible and resource-efficient, ready for scalable and extendable complex system integration.

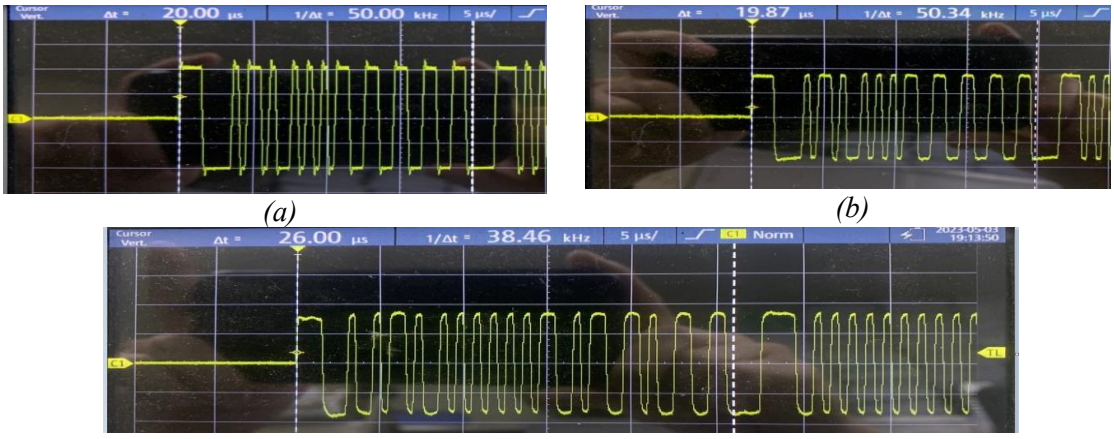
3.2. Signal quality survey

The physical layer signal quality survey is carried out by directly measuring the differential

signal on the transmission line with an oscilloscope, in order to verify compliance with the technical characteristics of the MIL-STD-1553B standard and to evaluate the effect of the extended Hamming code on the transmission frame. The experiment compared the signal between three subjects: the TX1-MP commercial module of Elcus, the self-designed module according to the basic standard, and the optimized self-designed module integrating BRAM and Hamming code.

Regarding the encoding format and time: The measurement results show that the waveform obtained from both the commercial module (Figure 8a) and the self-designed modules (Figure 8b,c) all comply with the Manchester II encoding standard, with a voltage level transfer characteristic at the midpoint of the bit cycle.

The measurement results show that all three modules (Figure 8) comply with the Manchester II encoding standard, with a level transition at the midpoint of the bit cycle. The transfer time of a data frame of the TX1-MP module and the basic self-designed module is approximately 20 µs, which is in line with the MIL-STD-1553B standard theory. For the Hamming code integrated module, the transmission time was increased to approximately 26 µs due to the addition of test bits; the waveform remained stable, with no significant distortion or noise. The differential signal amplitude of the self-designed module is about 9V, which is about 1V lower than that of commercial modules but still within the standard's permissible limits. The experimental results confirm that the self-designed FPGA module accurately reproduces physical signals according to the MIL-STD-1553B standard. The integration of Hamming codes increases the transmission frame length without affecting signal quality, proving the feasibility of a solution to improve reliability at the physical layer.



(a) *(b)*

(c)

Figure 8. *The signal on the MIL-STD-1553B bus of (a) the Elcus TX1-MP module, (b) the self-designed module, and (c) the optimized BRAM with incorporated Hamming codes.*

3.3. Verification of error detection and correction mechanisms

To evaluate the effectiveness of the integrated extended Hamming code algorithm on FPGAs, the verification process was performed using the Integrated Logic Analyzer (ILA) tool in Vivado, which allows for real-time direct observation of register status, Syndrome values, and error flags. The test system uses an error simulation block inserted into the transmission line to simulate noise, with three scenarios of single-bit error, double-bit error, and multi-bit error.

Experimental results show that, in the case of a single-bit error (Figure 9), the decoder computes a non-zero Syndrome value indicating the exact error position. Once the ERR_1bit signal is asserted, the system automatically corrects the corrupted data by inverting the bit at the location specified by the Syndrome within the same processing cycle. The corrected data (DATA_CORRECT) is then forwarded without requiring retransmission. For double-bit errors (Figure 10), the system detects the

fault but does not attempt correction. Instead, an error flag is activated to request retransmission, preventing the use of invalid data. Where a three-bit error indicates the theoretical limit of the extended Hamming code, at which the system can misidentify and correct the error incorrectly. However, the probability of this scenario happening in reality is very low.

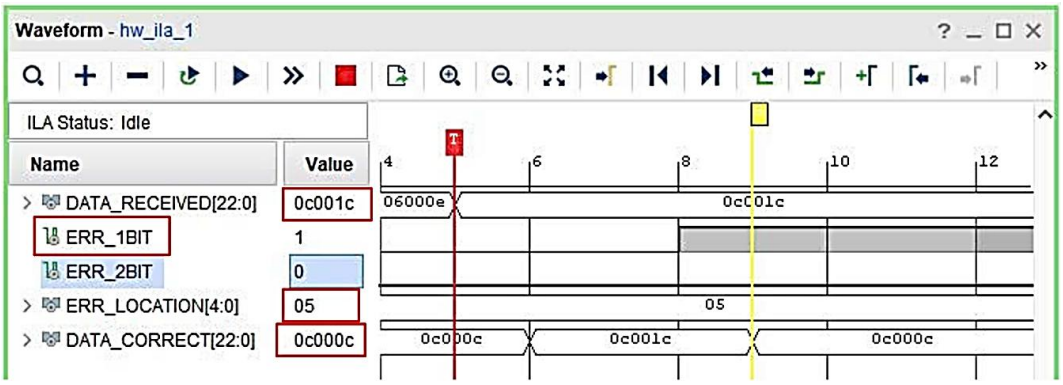


Figure 9. *1-bit error data read-write process on ILA.*

Compared with the traditional parity test mechanism of the MIL-STD-1553B standard, the proposed solution completely overcomes the possibility of missing double faults. Error detection and correction are performed instantaneously on the FPGA, without any degradation on system performance, except for an increase of approximately 6 μs per transmission frame due to the addition of test bits.

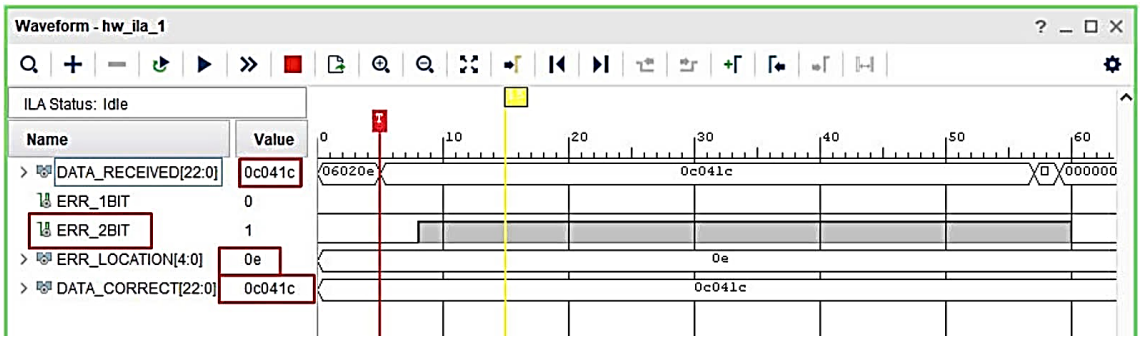


Figure 10. *The process of reading and writing 2-bit error data on ILA.*

3.4. Multi-protocol transmission and integration results

This section evaluates the module's ability to operate synchronously in a multi-standard integrated environment, focusing on verifying the two-way data flow between the host computer and the FPGA module. Control data is packaged as an Ethernet frame and transmitted to the FPGA, where it is decoded, separated, and distributed to the MIL-STD-1553B, ARINC-429, and RS-422 channels. The test results show that the input data is structured, accurately separated by each function card.

On the transmitter side, the MIL-STD-1553B BC1 case demonstrates proper division of a large data packet into two consecutive transmission sessions (CMD_1 and CMD_2), followed by corresponding status responses (STA_1 and STA_2). The waveform confirms correct timing, frame structure, and synchronization (Figure 11). The RS-422 channel accurately handles variable-length packets, while the ARINC-429 channel transmits and acquires full, stable data through dedicated TX/RX blocks.

In the opposite direction, the system collects data from multi-protocol sensors simultaneously, stores it through intermediate buffers, and aggregates it into a single Ethernet frame to send to the

computer. Experimental results show that the data obtained are 100% consistent with the source data, there is no packet loss or channel mixing, and the system maintains stable operation in real time even when the load changes.

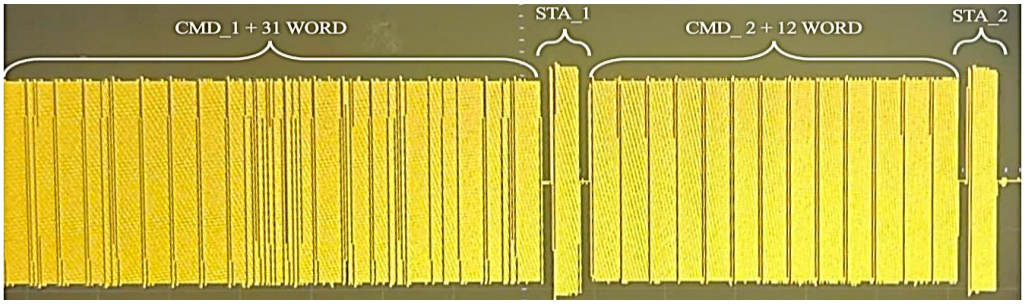


Figure 11. *MIL-STD-1553B signal measured on the BC1 card's transmission.*

Overall, the results confirm that the design module meets the requirements of bidirectional transmission, accurately converts between Ethernet and MIL-STD-1553B, ARINC-429, and RS-422 standards, ensuring synchronization, reliability, and applicability in military ship control systems.

4. CONCLUSIONS

This paper presents an FPGA-based multi-protocol data acquisition module integrating MIL-STD-1553B, ARINC-429, and RS-422 interfaces within a unified architecture. The system supports real-time acquisition, normalization, and aggregation of heterogeneous sensor data and delivers the processed information to a central monitoring system via a single Ethernet interface. Experimental results confirm stable operation, high reliability, and signal quality comparable to commercial solutions. A principal contribution of this work is the integration of an extended Hamming code into the MIL-STD-1553B communication module, enabling automatic single-bit error correction and double-bit error detection, while replacing external memory with on-chip BRAM to reduce latency and improve robustness. The proposed design demonstrates strong potential for deployment in mission-critical and domestically developed military electronic systems.

REFERENCES

[1]. U.S. Department of Defense, *"MIL-STD-1553B Aircraft Internal Time Division Command/Response Multiplex Data Bus"*, USA, (1978).
[2]. Texas Instruments, *"RS-422 and RS-485 Standards Overview and System Configurations"*, Dallas, TX, USA, (2010).
[3]. Sital Technology, *"ARINC-429 IP Core User's Manual"*, France, (2019).
[4]. J. Jose and S. Varghese, *"Design of 1553 Protocol Controller for Reliable Data Transfer in Aircrafts"*, 2012 12th International Conference on Intelligent Systems Design and Applications (ISDA), pp. 686–691, (2012).
[5]. C. Xin, X. Liang, S. Lv, Z. Lv, and T. Ma, *"Design and implementation of 1553B module communication system based on FPGA"*, Journal of Computing and Electronic Information Management, pp. 1–5, (2023).
[6]. Xilinx Inc., *"7 Series FPGAs Memory Resources"*, San Jose, CA, USA, (2019).
[7]. AMD, *"Block RAM Introduction"*, (2023).
[8]. R. W. Hamming, *"Error Detecting and Error Correcting Codes"*, Bell System Technical Journal, pp. 147–160, (1950).
[9]. AIM GmbH, *"ARINC 429 Specification Tutorial"*, Freiburg, Germany, (2019).
[10]. U. K. Kumar and B. S. Umashankar, *"Improved Hamming Code for Error Detection and Correction"*, IEEE International Conference, pp. 498–500, (2007).
[11]. N. V. Hung, N. N. Lam, N. V. Phuc and D. P. Hai Trang, *"Textbook of Data Transmission Techniques"*, Vietnam National University Press, Ho Chi Minh City, (2010).
[12]. Altium, *"How MIL-STD-1553B Standard Empowers Modern Defense Systems"*, (2023).

TÓM TẮT

Thiết kế mô-đun thu thập dữ liệu đa giao thức thời gian thực tập trung dựa trên FPGA cho các tàu chuyên dụng

Các mạng cảm biến được triển khai trên các phương tiện hiện đại hoạt động dưới nhiều giao thức truyền thông khác nhau và chịu các ràng buộc nghiêm ngặt về thời gian thực, do đó đặt ra yêu cầu cấp thiết về một giải pháp tập trung mang tính nhiệm vụ trọng yếu nhằm đảm bảo việc thu thập và tiền xử lý dữ liệu có tính xác định. Bài báo này trình bày thiết kế và triển khai một mô-đun thu thập và tái cấu trúc dữ liệu cảm biến dựa trên nền tảng FPGA, cho phép tích hợp đồng thời các giao diện MIL-STD-1553B, ARINC-429 và RS-422/485 trong một kiến trúc thống nhất. Độ tin cậy và khả năng chịu lỗi của hệ thống được nâng cao thông qua việc hỗ trợ các cơ chế mã sửa lỗi và sử dụng bộ nhớ trên chip có băng thông cao thay thế cho bộ nhớ ngoài truyền thống, qua đó đảm bảo hiệu năng xác định cho vận hành thời gian thực. Sau khi thu thập và chuẩn hóa, dữ liệu cảm biến được tổng hợp và truyền tới hệ thống giám sát trung tâm thông qua giao diện Ethernet tốc độ cao. Kết quả thực nghiệm xác nhận hệ thống hoạt động ổn định, cải thiện tính toàn vẹn dữ liệu và đáp ứng các yêu cầu xử lý thời gian thực trong các môi trường làm việc khắc nghiệt.

Từ khoá: FPGA; MIL-STD-1553B; Block RAM; Mã Hamming; Ethernet; ARINC-429.