

Modeling and control design of a non-ideal non-inverting buck–boost converter using a Type III compensator and logic switching

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Received 15 May 2026; Revised 09 Jul. 2026; Accepted 15 Sep. 2026; Published 15 Oct. 2026.

DOI: <https://doi.org/10.54939/1859-1043.j.mst.114.2026.30-37>

ABSTRACT

This paper proposes a unified modeling and control framework for a non-inverting DC–DC buck–boost (NIBB) converter operating under practical non-ideal conditions. A non-ideal small-signal model is developed by incorporating parasitic resistances and semiconductor voltage drops, enabling a more accurate representation of converter dynamics than conventional ideal models. The state-space averaging method is employed to derive the small-signal transfer functions for different operating modes. Based on the obtained model, a Type III compensator is systematically designed to improve phase margin, bandwidth, stability, and transient response. To ensure reliable operation over a wide input-voltage range, a hysteresis-based logic switch using Schmitt triggers is introduced to achieve smooth transitions among boost, buck–boost, and buck modes while preventing undesired frequent switching near transition boundaries. The proposed approach is validated through Software-in-the-Loop (SIL) simulations in the MATLAB/Simulink environment. Simulation results demonstrate stable voltage regulation, smooth mode transitions, and enhanced dynamic performance under varying operating conditions and load disturbances.

Keywords: Non-ideal DC–DC buck–boost converter; State-space averaging technique; Leverrier’s algorithm; Type III compensator; Small-signal modeling; Hysteresis logic switch.

1. INTRODUCTION

DC–DC converters are widely employed in renewable energy systems, battery energy storage systems (BESS), electric vehicles (EVs), and industrial power supplies to provide regulated voltage conversion under varying operating conditions [1, 2]. Among various converter topologies, the non-inverting buck–boost (NIBB) converter has attracted considerable attention because it can both step up and step down the input voltage while maintaining positive output polarity, making it suitable for applications with wide input-voltage variations [3].

In practical implementations, converter performance is significantly affected by parasitic resistances, capacitor equivalent series resistance (ESR), and semiconductor voltage drops, which alter the converter dynamics and may degrade controller performance if neglected during modeling [4–6]. Moreover, the presence of a right-half-plane (RHP) zero in continuous conduction mode (CCM) fundamentally limits the achievable control bandwidth of boost-derived converters, making conventional PI/PID controllers inadequate for fast transient response and robust stability [7–9]. Consequently, accurate non-ideal modeling together with appropriate frequency-domain controller design remains an important research topic.

Recent studies have focused on improving converter modeling and control under practical operating conditions. Lam et al. [10] proposed a non-ideal small-signal model with a Type III compensator for a DC–DC Ćuk converter, while Nguyen et al. [11] developed a frequency-domain cascaded-loop controller for a non-inverting buck–boost converter. In addition, recent studies published in the Journal of Military Science and Technology have investigated digital control, converter modeling, and battery energy conversion techniques, highlighting the increasing interest in practical implementation and dynamic performance enhancement [12–14]. Nevertheless, smooth transitions among boost, buck–boost, and buck operating modes remain insufficiently

addressed, particularly under wide input-voltage variations where frequent mode switching may degrade transient performance and converter reliability.

The research contribution of this paper is a unified modeling and control framework for a non-ideal NIBB converter. A non-ideal state-space averaged model incorporating parasitic resistances and semiconductor voltage drops is first developed. Based on this model, a Type III compensator is systematically designed to improve phase margin, bandwidth, and transient response. Furthermore, a Schmitt-trigger-based hysteresis logic switch is introduced to ensure smooth transitions among boost, buck–boost, and buck operating modes while suppressing undesired switching near transition thresholds. The proposed approach is validated through Software-in-the-Loop (SIL) simulations in MATLAB/Simulink, demonstrating stable voltage regulation and improved dynamic performance over a wide operating range.

2. MODELLING OF NON-IDEAL NON-INVERTING DC-DC BUCK-BOOST CONVERTER

The non-ideal non-inverting buck–boost (NIBB) converter combines buck and boost functions to achieve both step-up and step-down voltage conversion while maintaining positive output polarity [11]. Owing to its two duty cycles, the converter operates in three modes, namely buck, boost, and buck–boost, as summarized in Table 1. The converter configuration is shown in Figure 1, and its operation is analyzed under continuous conduction mode (CCM).

The converter operates in three switching states: Mode I (S1 ON, S2 ON), Mode II (S1 ON, S2 OFF), and Mode III (S1 OFF, S2 OFF) [12]. The resulting small-signal transfer functions used for controller design are presented below.

Table 1. Operating modes of NIBB converter [11].

Mode of operation	D_1	D_2
Buck	0 to 1	0
Boost	1	0 to 1
Buck-Boost	0 to 1	0 to 1 and always $D_2 < D_1$

Table 2 summarizes the operating points for the three converter modes: Buck ($V_{in} > V_{out}$), Boost ($V_{in} < V_{out}$), and Buck–Boost ($V_{in} \approx V_{out}$). Due to parasitic losses and semiconductor voltage drops, the non-ideal converter requires a higher duty cycle than the ideal model, particularly in Boost mode. These operating points are used for the design and evaluation of the proposed controller.

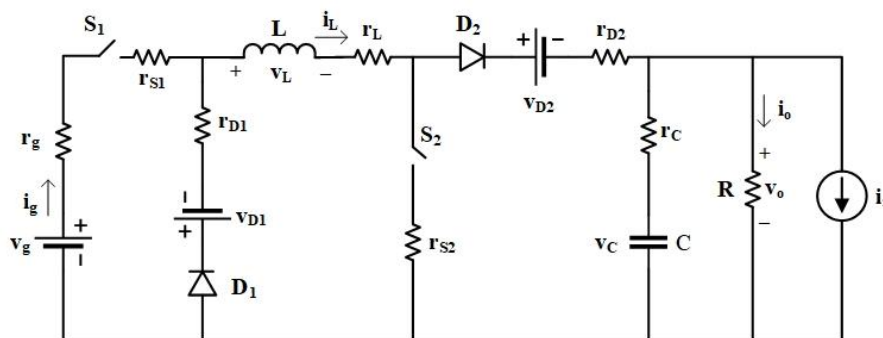


Figure 1. Circuit diagram of non-ideal non-inverting DC-DC Buck-boost converter.

The complete derivation of the nonlinear averaged model and the corresponding small-signal transfer functions has been reported in our previous study [14].

The duty cycle to output voltage transfer functions for buck and boost modes are given:

$$\text{Buck mode: } G_{vd1}(s) = \frac{3.6582 \times 10^3 s + 1.9053 \times 10^8}{s^2 + 1.8732 \times 10^3 s + 1.2814 \times 10^7} \quad (1)$$

$$\text{Boost mode: } G_{vd2}(s) = \frac{-0.0970 s^2 - 3.2205 \times 10^3 s + 9.5444 \times 10^7}{s^2 + 1.8959 \times 10^3 s + 6.0230 \times 10^6} \quad (2)$$

$$\text{Buck-Boost mode: } G_{vd1}(s) = \frac{1.7739 \times 10^3 s + 9.2392 \times 10^7}{s^2 + 1.6887 \times 10^3 s + 4.9756 \times 10^6} \quad (3)$$

$$G_{vd2}(s) = \frac{-0.1070 s^2 - 3.9142 \times 10^3 s + 8.6345 \times 10^7}{s^2 + 1.6887 \times 10^3 s + 4.9756 \times 10^6} \quad (4)$$

Due to higher conduction losses in the Buck–Boost mode, separate small-signal transfer functions are employed for the Buck, Boost, and Buck–Boost operating modes. The corresponding steady-state duty cycles are summarized in Table 2.

The converter parameters corresponding to the circuit of Figure 1 are listed below:

$$r_g = 0.3 \, \Omega, L = 500 \, \mu\text{H}, r_L = 0.34 \, \Omega, C = 160 \, \mu\text{F}, r_C = 0.12 \, \Omega$$

$$v_{fd1} = v_{fd2} = 0.5 \, \text{V}, r_{d1} = r_{d2} = 0.03 \, \Omega, r_{s1} = r_{s2} = 0.05 \, \Omega, f = 20 \, \text{kHz}, R = 22 \, \Omega/100 \, \text{W}$$

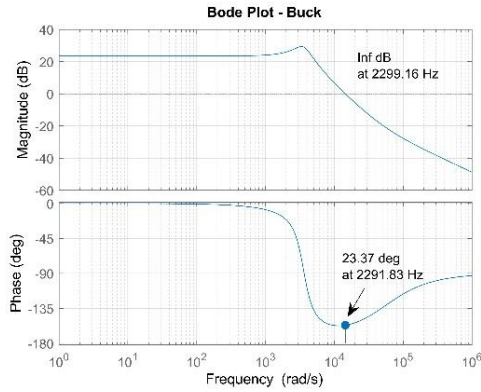


Figure 2. Bode plots of $G_{vd1}(s)$ for Buck mode.

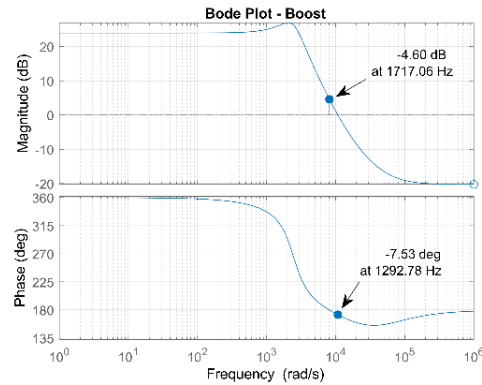


Figure 3. Bode plots of $G_{vd2}(s)$ for Boost mode.

Table 2. Steady-state duty cycles D_1 and D_2 for buck and boost modes.

Mode of operation	D_1	D_2
Buck ($v_o = 12 \, \text{V}$, $v_{in} = 15 \, \text{V}$)	0.490 1	0
Boost ($v_o = 12 \, \text{V}$, $v_{in} = 12 \, \text{V}$)	1	0.271
Buck-Boost ($v_o = 12 \, \text{V}$, $v_{in} = 9 \, \text{V}$)	0.695 7	0.391 5

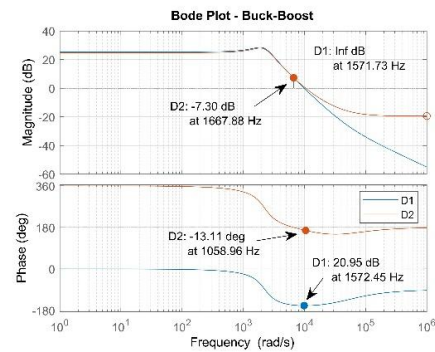


Figure 4. Bode plots of $G_{vd1}(s)$ and $G_{vd2}(s)$ for Buck-Boost mode.

The Bode plots in Figures 2–4 show that the Buck mode is stable, whereas the Boost and Buck–Boost modes exhibit poor stability margins due to the presence of a right-half-plane (RHP) zero. Consequently, the uncompensated converter cannot ensure reliable closed-loop operation, indicating the need for a Type III compensator.

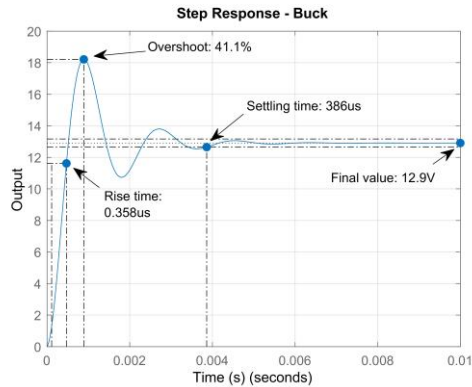


Figure 5. Step response of $G_{vd1}(s)$ for Buck mode.

The open-loop step responses in Figures 5–7 further confirm these limitations. The Buck mode exhibits large overshoot and oscillations, the Boost mode diverges rapidly, and the Buck–Boost mode shows an underdamped response under the D1 configuration but instability under the D2 configuration. These results demonstrate that the uncompensated converter cannot provide satisfactory voltage regulation, thereby justifying the use of the proposed Type III compensator.

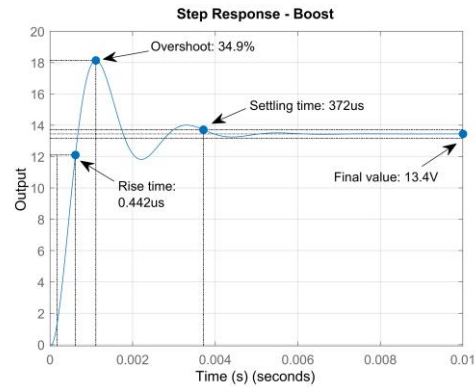


Figure 6. Step response of $G_{vd2}(s)$ for Boost mode.

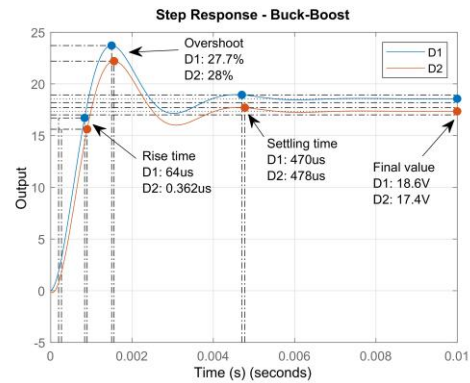


Figure 7. Step response of $G_{vd1}(s)$ and $G_{vd2}(s)$ for Buck-Boost mode.

3. CONTROLLER DESIGN FOR NON-IDEAL NON-INVERTING BUCK-BOOST CONVERTER

3.1. Type III compensator

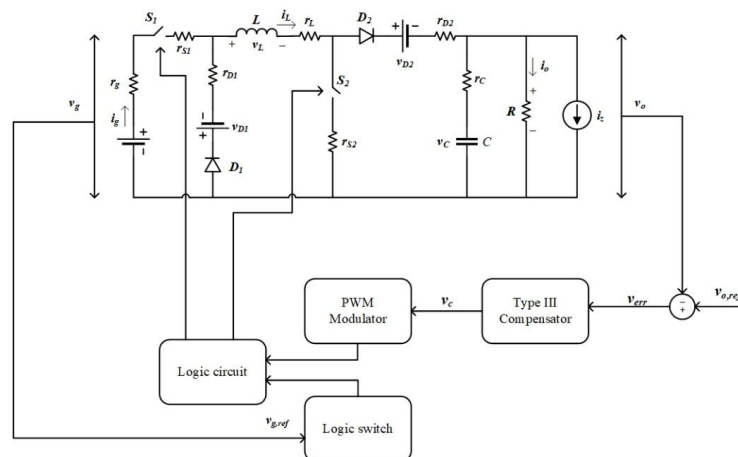


Figure 8. Schematic of controller for non-ideal NIBB converter.

Frequency-domain design is adopted because the switching frequency significantly affects the performance of the non-ideal NIBB converter. In this approach, phase margin (PM) and bandwidth

are the primary indicators of system stability and dynamic response. The closed-loop control structure is shown in Figure 8, where the output-voltage error is processed by a Type III compensator to improve phase margin, increase bandwidth, and enhance transient performance.

The compensated signal is then applied to the PWM modulator and logic circuit to generate suitable gate-driving signals for each operating mode. As a result, the proposed control system achieves stable voltage regulation, reduced oscillation, and improved dynamic performance over a wide operating range. The following steps are used to design the Type III compensator.

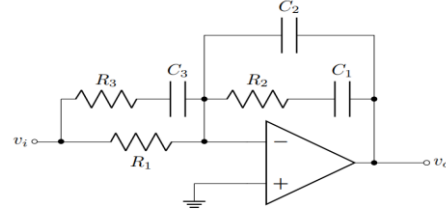


Figure 9. Type III error amplifier configuration with six passive components, three poles (including one at the origin), and two zeros.

To ensure a sufficient trade-off between fast transient response, high-frequency noise attenuation and to achieve the desired phase margin of 60 deg, the target crossover frequencies are selected as Buck ($f_c = 600 \text{ Hz}$), Boost ($f_c = 450 \text{ Hz}$), Buck/Boost ($f_c = 370 \text{ Hz}/420 \text{ Hz}$), which are approximately $\frac{1}{10}$ to $\frac{1}{20}$ of the switching frequency f_{sw} .

The complete design procedure of the Type III compensator has been presented in our previous work [13]. Therefore, only the final compensator transfer functions used in this study are summarized here.

$$\text{Buck mode: } G_{Cbuck}(s) = \frac{2.9044 \times 10^{-7} s^2 + 0.0011s + 1}{6.5361 \times 10^{-10} s^3 + 8.7157 \times 10^{-6} s^2 + 0.0291s} \quad (5)$$

$$\text{Boost mode: } G_{Cboost}(s) = \frac{7.0826 \times 10^{-7} s^2 + 0.0017s + 1}{9.0921 \times 10^{-3} s^3 + 1.1101 \times 10^{-5} s^2 + 0.0339s} \quad (6)$$

$$\text{Buck-Boost mode: } G_{Cd1}(s) = \frac{7.2559 \times 10^{-7} s^2 + 0.0017s + 1}{2.5018 \times 10^{-9} s^3 + 1.9883 \times 10^{-5} s^2 + 0.0395s} \quad (7)$$

$$G_{Cd2}(s) = \frac{8.9968 \times 10^{-7} s^2 + 0.0019s + 1}{1.1637 \times 10^{-9} s^3 + 1.4093 \times 10^{-5} s^2 + 0.0427s} \quad (8)$$

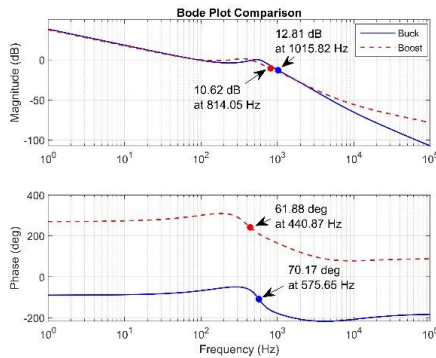


Figure 10. Bode plot of buck mode and boost mode after compensation.

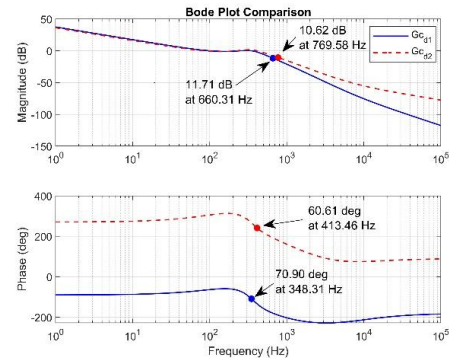


Figure 11. Bode plot of buck-boost mode after compensation.

The Bode plots in Figures 10 and 11 demonstrate that the proposed Type III compensator significantly improves the frequency response of the non-ideal NIBB converter by compensating for the phase lag introduced by the LC resonant pole pair. In all operating modes, the compensated system achieves positive gain and phase margins with the desired crossover frequencies, indicating robust closed-loop stability. In particular, the Boost and Buck–Boost modes exhibit substantially improved phase margins and bandwidth, resulting in enhanced dynamic performance and reliable

operation over a wide operating range.

The closed-loop step responses in Figures 12 and 13 demonstrate the effectiveness of the proposed Type III compensator. All operating modes achieve stable, non-oscillatory responses with zero overshoot and converge accurately to the 12 V reference without steady-state error. Although the transient response is slightly moderated to compensate for the right-half-plane (RHP) zero and low-damping characteristics, the proposed controller ensures robust stability and satisfactory dynamic performance.

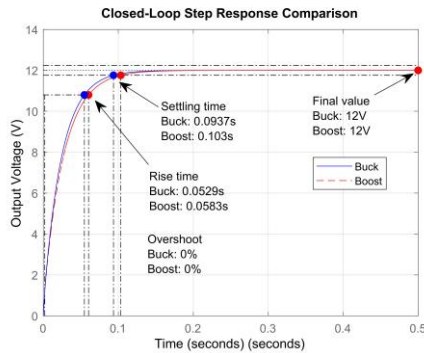


Figure 12. Step response of buck mode and boost mode after compensation.

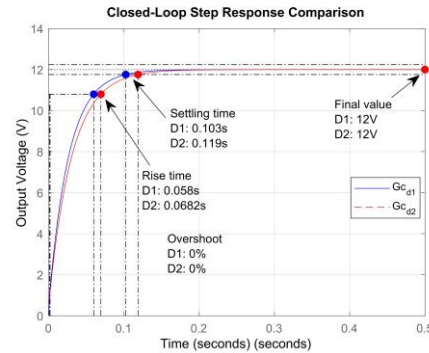


Figure 13. Step response of buck-boost mode after compensation.

Table 3. Time-domain performance metrics of open-loop and closed-loop systems.

Operating mode	Control configuration	System stage	Rise time	Settling time	Peak overshoot	Final value
Buck	$G_{C\text{buck}}$	Open-loop	$0.358 \mu\text{s}$	$386 \mu\text{s}$	41.1%	12.9 V
		Closed-loop	0.0529 s	0.0937 s	0%	12.0 V
Boost	$G_{C\text{boost}}$	Open-loop	$0.442 \mu\text{s}$	$372 \mu\text{s}$	34.9%	13.4 V
		Closed-loop	0.0583 s	0.1030 s	0%	12.0 V
Buck-Boost	G_{Cd1} - G_{Cd2}	Open-loop	$64.0 \mu\text{s}/$ $0.362 \mu\text{s}$	$470 \mu\text{s}/$ $478 \mu\text{s}$	$27.7\%/$ 28.0%	$18.6 \text{ V}/$ 17.4 V
		Closed-loop	0.0588 s/ 0.0682 s	0.1030 s/ 0.1190 s	0%	12.0 V

3.2. Logic switch

The converter operating mode is selected according to the input voltage. For a regulated output of 12 V, Boost, Buck–Boost, and Buck modes are activated when $V_{in} < 11 \text{ V}$, $11 \leq V_{in} \leq 13 \text{ V}$, and $V_{in} > 13 \text{ V}$, respectively. To suppress chattering near the transition boundaries, a Schmitt-trigger-based hysteresis logic is adopted with thresholds of 11/10.5 V and 13/12.5 V, providing stable mode transitions under input-voltage fluctuations.

A Schmitt trigger is a hysteresis comparator with two threshold voltages: the upper threshold (VUT) and the lower threshold (VLT). The output changes state only when the input crosses these thresholds, providing immunity against noise-induced switching. As shown in Figure 14, the proposed logic switch employs two Schmitt triggers driven by the converter input voltage. The upper thresholds are determined by the voltage dividers RV1 and RV2, while the lower thresholds are adjusted by resistors R1, R2, R4, and R5.

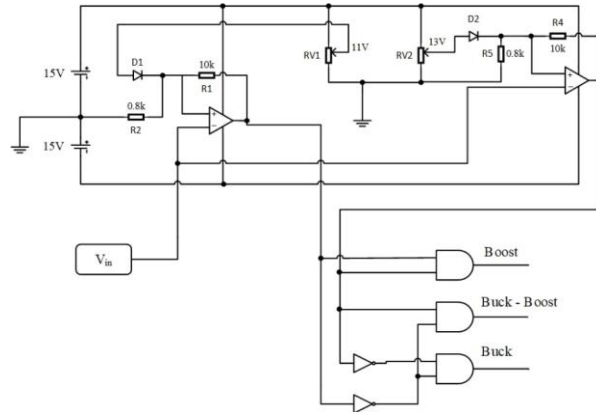


Figure 14. Schematic of the logic switch.

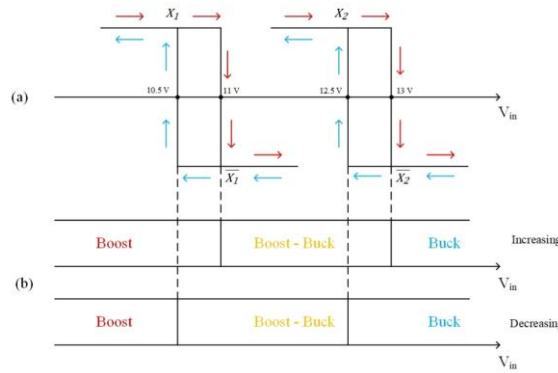


Figure 15. Hysteresis characteristics of the logic switch and corresponding operating mode transitions.

The output signals of the Schmitt triggers are denoted as x_1 and x_2 , respectively. The input–output characteristics of the Schmitt triggers corresponding to the increasing and decreasing input voltage processes are illustrated in Figure 15(a). The relationship between the input signal and the output signals of the logic switch is presented in Table 4. From Table 4 we got: $F_{boost} = x_1 \cdot x_2$; $F_{buck/boost} = \overline{x_1} \cdot x_2$; $F_{buck} = \overline{x_1} \cdot \overline{x_2}$

Table 4. Truth table of the operating mode selection logic				
x_1	x_2	F_{boost}	$F_{buck/boost}$	F_{buck}
0	0	0	0	1
0	1	0	1	0
1	0	x	x	x
1	1	1	0	0

The output signals of the logic switch during increasing and decreasing input voltage conditions are shown in Figure 15(b). The output signals of the logic switch are then combined with the PWM signals and applied to the MOSFETs of the converter.

4. CONCLUSIONS

This paper has presented a control strategy for a non-ideal non-inverting buck–boost (NIBB) converter based on previously developed small-signal models. A Type III compensator and a Schmitt-trigger-based hysteresis logic switch were employed to improve system stability, dynamic performance, and mode-transition reliability.

The proposed approach was validated through Software-in-the-Loop (SIL) simulations in the MATLAB/Simulink environment. The results demonstrated stable output-voltage regulation,

smooth transitions among operating modes, and improved dynamic performance over a wide operating range. The proposed control strategy provides a practical solution for enhancing the stability and reliability of non-ideal NIBB converters and can serve as a basis for future hardware implementation and experimental validation.

REFERENCES

- [1]. M. H. Rashid, “*Power Electronics: Circuits, Devices, and Applications*”, 4th ed., Upper Saddle River, NJ, USA: Pearson, (2014).
- [2]. R. W. Erickson and D. Maksimović, “*Fundamentals of Power Electronics*”, 2nd ed., Boston, MA, USA: Springer, (2001).
- [3]. F. L. Luo and H. Ye, “*Advanced DC/DC Converters*”, Boca Raton, FL, USA: CRC Press, (2004).
- [4]. R. D. Middlebrook and S. Čuk, “*A general unified approach to modelling switching-converter power stages*”, in Proc. IEEE Power Electron. Spec. Conf., pp. 18–34, (1976).
- [5]. V. Vorperian, “*Simplified analysis of PWM converters using model of PWM switch. Part I: Continuous conduction mode*”, IEEE Trans. Aerosp. Electron. Syst., vol. 26, no. 3, pp. 490–496, (1990).
- [6]. B. Bryant and M. K. Kazimierzczuk, “*Voltage-loop power-stage transfer functions with MOSFET delay for boost PWM converter operating in CCM*”, IEEE Trans. Ind. Electron., vol. 54, no. 1, pp. 347–353, (2007).
- [7]. K. Ogata, “*Modern Control Engineering*”, 5th ed., Upper Saddle River, NJ, USA: Prentice Hall, (2010).
- [8]. C. Basso, “*Designing Control Loops for Linear and Switching Power Supplies*”, Norwood, MA, USA: Artech House, (2012).
- [9]. C. K. Tse, “*Complex Behavior of Switching Power Converters*”, Boca Raton, FL, USA: CRC Press, (2003).
- [10]. V. T. Lam et al., “*Modeling and Control Designing for Non-Ideal DC–DC Čuk Converter Using Type III Compensator*”, in Advances in Engineering Research and Application, LNNS, vol. 1804, Cham, Switzerland: Springer, pp. 315–327, (2026).
- [11]. D. T. Nguyen, D. N. Nguyen, D. H. Luu, and C. D. Nguyen, “*Frequency-domain based design and modeling of a cascaded-loop controller for a non-ideal non-inverting buck–boost DC–DC converter*”, in Advances in Engineering Research and Application, LNNS, vol. 1803, Cham, Switzerland: Springer, (2026).
- [12]. N. Q. Minh, C. T. Trung, and H. Anh, “*Modeling of grid-connected inverter using grid-forming technology*”, Journal of Military Science and Technology, FEE 2024, pp. 51–57, (2024).
- [13]. N. V. Thuy and N. V. Chi, “*Design of energy balancing circuit for battery cells connected in series based on modifying the bidirectional Čuk converter*”, Journal of Military Science and Technology, FEE 2024, pp. 58–64, (2024).
- [14]. T. X. Dinh, N. N. Tuan, N. N. Tien, D. N. Khang, N. D. Long, and P. V. Phu, “*Optimal power management for hybrid electrical vehicle*”, Journal of Military Science and Technology, vol. 97, pp. 16–24, (2024).

TÓM TẮT

Mô hình hóa và thiết kế điều khiển bộ biến đổi Buck–Boost không đảo cực tính có xét đến các yếu tố phi lý tưởng, sử dụng bộ bù Type III và logic chuyển chế độ

Bài báo đề xuất một khung mô hình hóa và điều khiển thống nhất cho bộ biến đổi DC–DC buck–boost không đảo cực tính (NIBB) trong điều kiện phi lý tưởng. Mô hình tín hiệu nhỏ được xây dựng bằng phương pháp trung bình hóa không gian trạng thái, có xét đến điện trở ký sinh và sụt áp trên các linh kiện bán dẫn nhằm phản ánh chính xác đặc tính động của bộ biến đổi. Trên cơ sở mô hình này, bộ bù Type III được thiết kế để nâng cao dự trữ pha, băng thông, độ ổn định và đáp ứng quá độ của hệ thống. Đồng thời, một mạch chuyển đổi logic sử dụng Schmitt trigger được đề xuất nhằm thực hiện chuyển đổi mượt giữa các chế độ boost, buck–boost và buck, đồng thời loại bỏ hiện tượng chuyển mạch liên tục tại các vùng chuyển tiếp. Phương pháp được kiểm chứng bằng mô phỏng Software-in-the-Loop (SIL) trên nền tảng MATLAB/Simulink. Kết quả cho thấy hệ thống duy trì điều chỉnh điện áp ổn định, chuyển đổi chế độ êm và cải thiện đáng kể đặc tính động dưới các điều kiện thay đổi điện áp đầu vào và tải.

Từ khóa: Bộ biến đổi DC–DC buck–boost phi lý tưởng không đảo cực tính; Phương pháp trung bình hóa không gian trạng thái; Thuật toán Leverrier; Bộ bù Type III; Mô hình tín hiệu nhỏ; Mạch chuyển đổi logic có đặc tính trễ.