A 1.8 to 4 GHz inductor-less highly linear CMOS LNA for wire-less receivers

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ABSTRACT

This paper presents an inductor-less wide-band highly linear low-noise amplifier (LNA) for wire-less receivers. The inductor-less LNA consists of a complementary current-reuse common source amplifier combined with a low-current active feedback to obtain wide range input impedance matching and low noise figure. In our LNA, a degeneration resistor is utilized to improve linearity of the LNA. Furthermore, we designed a bypass mode for the LNA to extend the range of its applications. The proposed LNA is implemented in 28 nm CMOS process. It has a gain of 14.9 dB and a bandwidth of 2.2 GHz. The noise figure (NF) is 1.95 dB and the third-order input intercept point (IIP3) is 24.8 dBm at 2.3 GHz. It consumes 17.2 mW at a 0.9-V supply and has an area of 0.011 mm^2.

Keywords: Inductor-less; Current-reuse; Active feedback; Wide-band; High linearity; Low noise amplifier.

1. INTRODUCTION

Nowadays, many wireless communication standards in different frequency bands have been developed for various communication applications such as 3rd generation mobile communication system (3G), long-term evolution (LTE), 5G, wire-less fidelity (Wi-Fi) and Bluetooth. Therefore, broadband receivers have become mainstream to use for mixing various standards [1-3]. In these receivers, the low noise amplifier (LNA) is an important component which plays a key role for front-end block. The wide-band LNA should satisfy some requirements, involving low noise figure (NF), great input impedance matching and high linearity. So far, many noise canceling schemes of the LNA have been implemented to achieve simultaneous wideband and low noise but not high linearity [4, 5]. Therefore, the most significant challenge of a LNA design is to ensure the linearity. The front-end of the LNA requests a high linearity to eliminate the intermodulation or cross-modulation due to the increased concurrency of adjacent blockers or transmitter on-chip leakage [6]. To overcome this challenge, a common source (CS) amplifier with current-reuse architecture and an active inductor for input matching are used in [7]. In [8], a parallel combination of common gate (CG) and CS amplifiers is realized and a resistive feedback structure is used to balance the multiple tradeoffs among NF, input matching and gain. The IIP3 in [7] and [8] obtained 5 dBm and 5.8 dBm, respectively. However, these LNAs employ an inductor in design. Consequently, the cost and die area will both be grown making these LNAs less attractive in practical applications. To overcome this problem, inductor-less LNAs are implemented in [9, 10]. These LNAs use current-reuse CS amplifier and active shunt-feedback to achieve high linearity of 12.4 dBm and 7.9 dBm in IIP3, respectively.

This paper proposes an improved version of the LNA introduced [9, 10]. By using a degeneration resistor, the linearity of the LNA is enhanced. The LNA simultaneously obtains wide-band, low NF and high linearity. In addition, a bypass mode for the LNA is adopted. This paper is organized as follows. Section II introduces the architecture of the proposed inductor-less LNA. Next, in Section III, the circuit implementation is described in detail. Section IV provides the experimental results on 28 nm CMOS process followed by conclusions in Section V.

2. PROPOSED ARCHITECTURE

The block diagram of the proposed differential inductor-less LNA is presented in fig.1. The LNA includes two modes: LNA mode and bypass mode. The selection of the working mode for the LNA is done by the digital control bit, *C*. When the signal strength at the receiver input is small, the control bit *C* is set to '0' to select the LNA mode for the amplifier. Conversely, when the received signal strength is large, the control bit is set to '1' to select the bypass mode for the amplifier and the received signal is applied directly to the mixer without going through the LNA circuit.

As depicted in fig. 1, capacitors C1 and C2 are used to block DC for the input and output of the LNA, respectively. In addition, C2 plays the role of matching between LNA and Mixer so the value of C2 must be chosen carefully when designing the complete front-end circuit with mixer following the LNA circuit. The proposed LNA employs degeneration resistor to improve the linearity of the circuit where the value of the resistor can be varied so that the circuit achieves a wide range of values of IIP3 to counteract the influence of process, voltage and temperature (PVT). To do this, four digital control bits B0-B3 are used to select the resistor value in the LNA circuit.

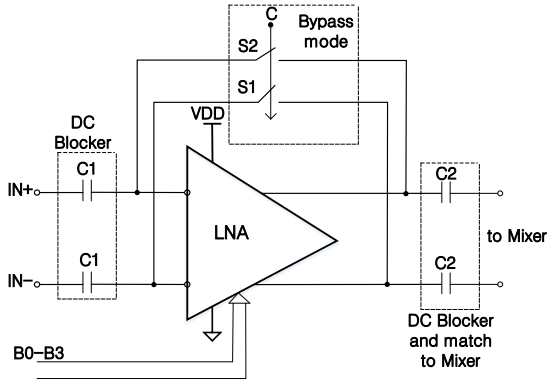

Figure 1. *Block diagram of the proposed inductor-less LNA.*

3. CIRCUIT DESCRIPTION

3.1. Proposed LNA

The proposed LNA is illustrated in fig. 2. It includes a main amplifier (A) and a shunt feedback path (F).

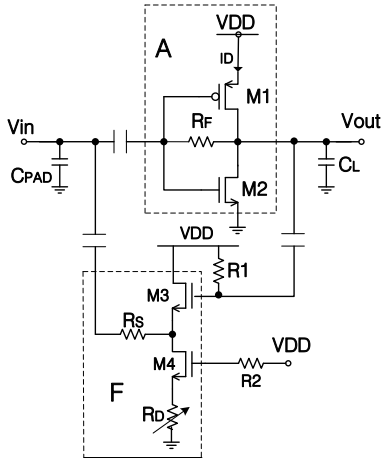

Figure 2*. Circuit implementation of the proposed LNA.*

The main amplifier bases on a current-reuse structure with PMOS and NMOS pairs connected in series. This is a self-bias structure in which PMOS and NMOS are biased by the D terminal voltage of M1 and M2 through the R_F resistor. By using current-reuse structure, transconductance is boosted and the LNA achieves high gain and low NF simultaneously. The active feedback loop using source follower structure enables a wideband matching and ensures a high linearity of the LNA. A degeneration resistor (R_D) which can be changed is added to enhance linearity of the LNA. The S terminal voltage of M1 and the bias voltage for M4 are connected to the power supply (VDD) of the LNA to eliminate the need for Band gap reference circuits outside of the LNA circuit. As a result, the total area occupied by the LNA circuit is reduced.

The circuit analysis in this section is performed based on [9] with the results summarized to serve the design of the LNA. The architecture of the LNA circuit in fig. 2 is modeled by fig. 3 for simplicity in calculating the formulas. In which G_{m1} and G_{m2} are transconductance of current-reuse structure (A) and source follower structure (F), respectively. Then, G_{m1} and G_{m2} are given by

$$G_{m1} = g_{m1} + g_{m2} \quad (1)$$

$$G_{m2} = \frac{g_{m3}}{1+g_{m3}R_S} \quad (2)$$

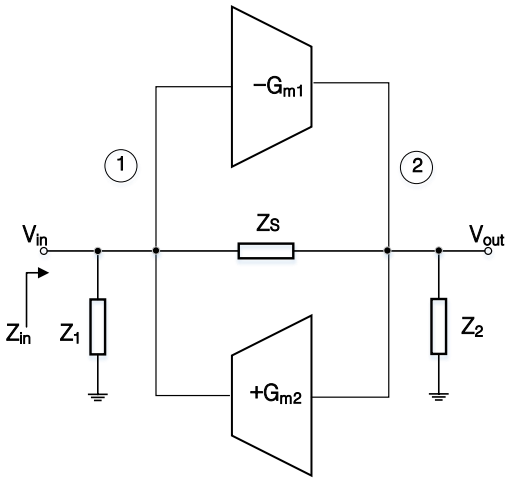

***Figure 3**. Modeling of LNA in fig. 2.*

The input parasitic impedance is:

$$Z_1 = \frac{1}{g_{ds3}+g_{ds4}} \left\| \frac{1}{s(C_{pad}+C_{gs2}+C_{sb3}+C_{db4})} \right. \quad (3)$$

Feedback structure's impedance is:

$$Z_S = R_F \left\| \frac{1}{s(C_{gd2}+C_{gs3})} \right. \quad (4)$$

Output impedance is:

$$Z_2 = \frac{1}{g_{ds2}} \left\| \frac{1}{s(C_L+C_{gd3}+C_{db2})} \right. \quad (5)$$

where g_{dsi} is output conductance of the device M_i; C_{gsi}, C_{gdi}, C_{dbi}, C_{sbi} are the intrinsic parasitic capacitances of device M_i; C_{pad} is the input pad capacitance and C_L is the load capacitance.

The voltage gain of the LNA is given by

$$A_V = -(G_{m1} - \frac{1}{Z_S})(Z_2||Z_S) \tag{6}$$

If $Z_S >> Z_2$, (6) is reduced to

$$A_V = -G_{m1}Z_2 \tag{7}$$

Expression (7) reveals that the gain of the LNA circuit strongly depends on the A stage.

The input impedance of the LNA is determined by

$$Z_{in} = \frac{Z_B+Z_2}{1+(G_{m1}-G_{m2}+G_{m1}G_{m2}Z_B)Z_2}||Z_1 \tag{8}$$

If the bias resistor R_F of block A is large enough and $g_{ds3} + g_{ds4} \approx 0$, then substituting (3), (4) and (5) in (8), the input impedance is calculated by the formula

$$Z_{in} \approx \frac{1+g_{m3}R_S}{g_{m3}(1+|A_V|)} \tag{9}$$

Expression (9) presents that wide-band input impedance matching could be achieved by adjusting and optimizing the gain (A_V), feedback resistor (R_S) and M3 transistor (g_{m3}) of the LNA. In which R_S must be chosen small enough to keep broadband impedance matching.

The main noise distribution of the LNA comes from the MOS devices (M1, M2, M3, M4), feedback resistor (R_S) and bias resistor (R_F). Noise factor of each element in block A can be expanded as

$$n_{M1} = \frac{\gamma_{1N}g_{m1}}{\alpha_1 G_{m1}^2}R_B\left[\frac{1}{R_B} + \frac{g_{m3}}{1+g_{m3}R_S}\right]^2 \tag{10}$$

$$n_{M2} = \frac{\gamma_{1P}g_{m2}}{\alpha_2 G_{m1}^2}R_B\left[\frac{1}{R_B} + \frac{g_{m3}}{1+g_{m3}R_S}\right]^2 \tag{11}$$

$$n_{R_F} = \frac{1}{R_F}\frac{R_B}{(1+g_{m3}R_S)^2} \tag{12}$$

And noise factor of each element in block F can be expanded as

$$n_{M3} = \frac{\gamma_2 g_{m3}}{\alpha_3}\frac{R_B}{(1+g_{m3}R_S)^2} \tag{13}$$

$$n_{M4} = \frac{\gamma_3 g_{m4}}{\alpha_4}\frac{R_B}{(1+g_{m3}R_S)^2} \tag{14}$$

$$n_{R_S} = R_S R_B\left[\frac{g_{m3}}{(1+g_{m3}R_S)^2}\right]^2 \tag{15}$$

where R_B is the signal source resistance, γ is the thermal noise excess factor, $\alpha = \frac{g_m}{g_{do}}$ and g_{do} is the output transconductance at V_{DS} = 0 V. Expressions (10-15) show that circuit A is the dominant noise component of the LNA [9]. As a result, a low-noise design for circuit A is required to achieve a low-noise LNA. This can be realized by choosing large bias resistors and large size of the MOS devices M1, M2.

3.2. Control IIP3 of LNA

Fig. 4 presents the implemented diagram of proposed IIP3 control circuit for the LNA. As mentioned early, a degeneration resistor is added into the feedback stage to enhance the linearity of the LNA. To achieve a wide range of values of IIP3, four digital control bits, B0, B1, B2, B3, are used in this work.

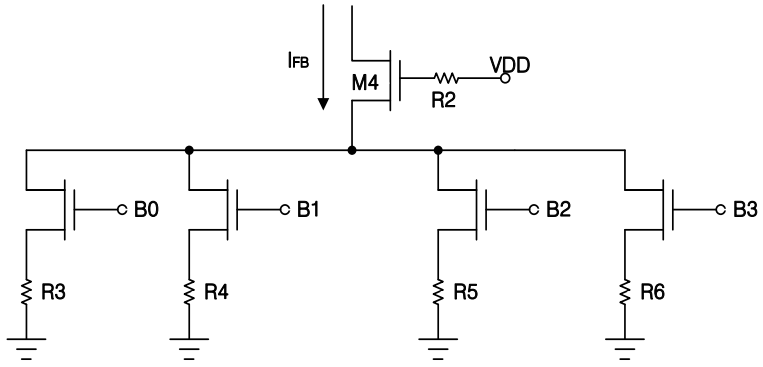

***Figure 4**. Control IIP3 by digital logic.*

Degeneration resistor values are selected when the control bit is high logic level and disconnected from the circuit when the control bit is low logic level. Therefore, the four control bits select 16 possible values of the degeneration resistor and respectively generate 16 feedback current values (table I) for the feedback stage. Feedback current value is designed from 0.08 mA to 1.2 mA with 80 µA linear increments. This is done by selecting the values R3, R4, R5, R6 so that the corresponding feedback current is 0.08 mA (B0 = 1, B1 = 0, B2 = 0, B3 = 0), 0.16 mA (B0 = 0, B1 = 1, B2 = 0, B3 = 0), 0.32 mA (B0 = 0, B1 = 0, B2 = 1, B3 = 0) and 0.64 mA (B0 = 0, B1 = 0, B2 = 0, B3 = 1). The size of the NMOSs for digital control must be not small to minimize their noise contribution to the whole circuit.

***Table I.** Feedback current values corresponding to the control bits.*

B3	B2	B1	B0	I_{FB} (mA)
0	0	0	1	0.08
0	0	1	0	0.16
0	0	1	1	0.24
0	1	0	0	0.32
0	1	0	1	0.4
0	1	1	0	0.48
0	1	1	1	0.56
1	0	0	0	0.64
1	0	0	1	0.72
1	0	1	0	0.8
1	0	1	1	0.88
1	1	0	0	0.96
1	1	0	1	1.04
1	1	1	0	1.12
1	1	1	1	1.2

3.3. Bypass mode

In this work, the LNA circuit with bypass mode is designed to increase its application range. A switch is used to make the bypass mode as shown in fig. 5. The mode selection for LNA is performed by switching the values of the digital control bit *C*.

C = ‘0’, select LNA mode;

C = ‘1’, select bypass mode.

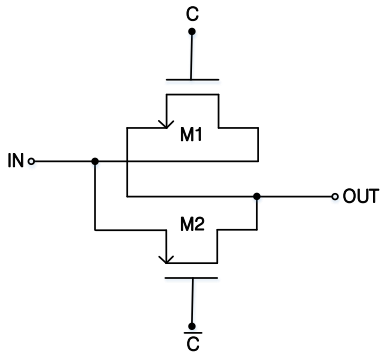

***Figure 5**. Switch circuit for bypass mode of the LNA.*

The switch designing must be executed carefully to both ensure the quality of the LNA circuit in bypass mode and does not affect the quality of the LNA circuit in the amplification mode.

3.4. LNA design process

After analyzing the circuit in Section A, in this Section, we present a design process for the proposed inductor-les LNA circuit. This process simplifies the design of the LNA and can be used as a reference for the design of other LNAs. There are 7 steps to design the LNA as follow.

Step 1: Design the block A in fig. 2. Select the widths of M1 and M2 (equal widths) to get large G_m (using formula (1)) and low NF (Equation 10-11). Choose a value of R_F large enough to ensure the gain and noise of the block A. Design M1 and M2 in the saturation region so that the circuit works stably under the influence of PVT.

Step 2: Connecting the block F with an ideal current source (to generate I_{FB}), the initialization value of I_{FB} is less than 1 mA to save power and reduce noise from the block F to the whole circuit. Then, select g_{m3} value and R_B value.

Step 3: Check the NF of the whole circuit. Reduce I_{FB} if NF does not meet the target. The I_{FB} must not be reduced too small because then the influence of the resistor Rs on the impedance matching will be limited. Change g_{m3} and Rs to perform impedance matching according to formula (9). Adjust the R_F resistor so that the gain is satisfactory. Test S_{11} with respect to the value of the R_F resistor. Because I_{FB} also affects S_{11}, R_B is preferred to achieve the target gain.

Step 4: Determine I_{FB}: Measure OIP3 and IIP3 to check that with the selected values for M1, M2, R_F of block A, in what range the I_{FB} will meet the requirements of IIP3, OIP3.

Step 5: Check again the impedance matching (S_{11}) when changing the I_{FB} because there is a constraint between the wideband matching and the linearity of the circuit. In step 3, if the reduction of I_{FB} is no longer reasonable, we increase G_{m1} to ensure that M1 and M2 are in the saturation region. Repeat from step 2 until NF and S_{11} reach the target.

Step 6: Replace the ideal current source by a digital control circuit to improve the linearity of the LNA.

Step 7: Design switch for bypass mode of the LNA. The switching circuit parameters are calculated carefully selected to optimize the quality of the LNA circuit in Bypass mode and LNA mode.

After following the steps in the LNA design, we obtain the values of the parameters in the LNA circuit as shown in table II.

***Table II.** Design parameter values in the LNA.*

M1	180µm/30µm	M2	180µm/30µm	M3	60µm/30µm
M4	45µm/30µm	R_F	4.1 kΩ	R_S	210 Ω

4. SIMULATION RESULTS AND DISCUSSION

Based on the previous analysis, a 1.8 to 4 GHz LNA is designed. The proposed differential inductor-less LNA is implemented in a 28 nm CMOS process. The layout picture of the LNA is presented in fig. 6. It occupies an area of 0.011 mm^2 without the Pads. The power consumption is 17.2 mW at the supply voltage of 0.9 V.

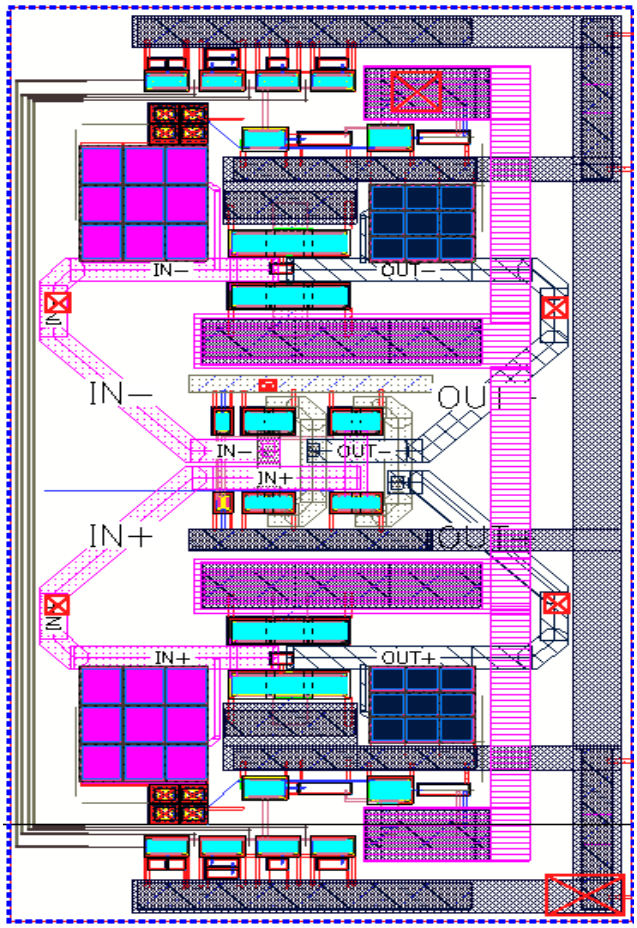

Figure 6. *Layout of the LNA.*

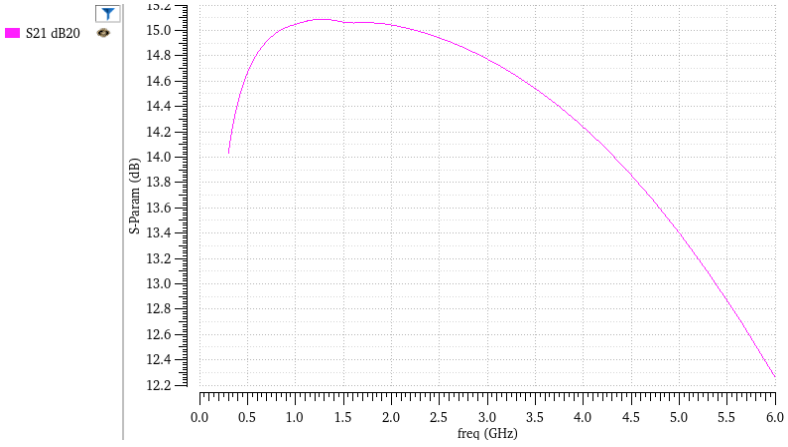

Figure 7*. Post-layout simulation result of* S_{21}.

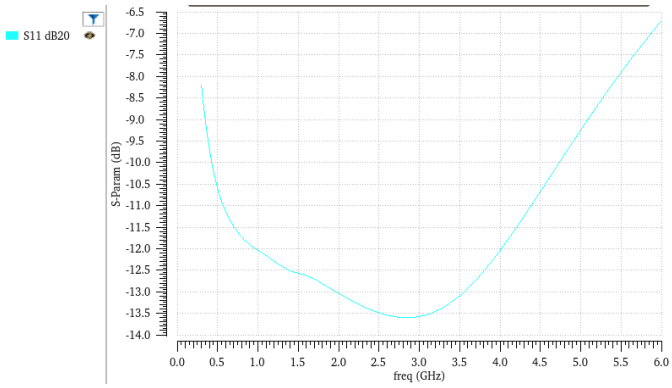

***Figure 8**. Post-layout simulation result of S_{11}.*

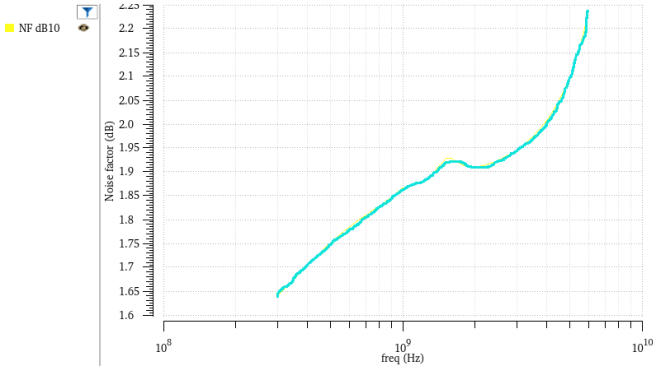

***Figure 9**. Post-layout simulation result of NF.*

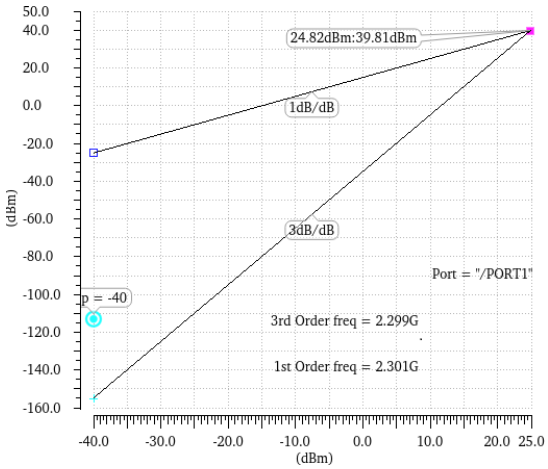

***Figure 10**. Post-layout simulation result of IIP3.*

Post-layout simulation results are depicted in fig.7 - fig.10. Fig. 7 shows the power gain (S_{21}) of the LNA. S_{21} is always greater than 14 dB in full operation range, 1.8 GHz – 4 GHz, and the flatness of the gain is approximately 0.06 dB per 100 MHz. This result shows that the proposed LNA architecture can be used in front-end circuits for direct conversion receivers where it requests wide baseband bandwidth as LTE or 5G. Input reflection coefficient (S_{11}) qualifies the input impedance matching and S_{11} is below -10 dB in the frequency band of interest as shown in fig. 8. Therefore, the LNA could obtain greatly input impedance matching. The lowest NF that LNA achieved is 1.65 dB as illustrated in fig. 9 and NF increases by 1.95 dB when the frequency reaches 4 GHz.

The third order interception point is measured in a two-tone manner. The two input signals are separated at 1 MHz away. Fig. 10 shows the IIP3 result. IIP3 obtains 24.8 dBm at 2.3 GHz. IIP3 performance can be controlled by bits B0-B3 to overcome the influence of the PVT. This result indicates that the addition of degeneration resistor to the feedback stage has considerably enhanced the linearity of the proposed LNA. Table III benchmarks the performances with the prior art. This work has low NF, high linearity with trade-off of power.

Table III. *Performance Comparison of LNA.*

	[7] (measure)	[9] (measure)	[11] (simulation)	**This work** (post-simulation)
Technology (nm)	130 CMOS	130 CMOS	110 CMOS	28 CMOS
Supply (V)	1.4	1.5	1.2	0.9
BW (GHz)	3.9	2	2	2.2
Inductor	Yes	No	No	No
S11 (dB)	< -10	< -10	< -10	< -10
S21 dB)	10.8	19.2	7.9	14.9
NF dB)	3.5	2.4	3.3	1.95
IIP3 (dBm)	-1.6	8.6	3.7	24.8
Area (mm^2)	0.18	0.014	N/A	0.011
Power (mW)	6.16	3.11	3.24	17.2

5. CONCLUSION

The proposed inductor-less LNA is implemented in 28 nm CMOS process. The LNA achieves wide-band, low-noise, smal gain variation across the working bandwidth and high linearity by combining current-reuse structure and active feedback structure. A degeneration resistor is added into the feedback structure to enhance IIP3 to 24.8 dBm in post-simulation, outperforming other published schemes. In future work, we will completely design a RF Front-end circuit for direct conversion receiver including proposed inductor-less LNA.

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TÓM TẮT

MẠCH CMOS LNA 1.8 ĐẾN 4 GHz TUYẾN TÍNH CAO KHÔNG SỬ DỤNG CUỘN CẢM CHO MÁY THU VÔ TUYẾN

Bài báo này trình bày về mạch khuếch đại tạp âm thấp (LNA) có độ tuyến tính cao, dải rộng, không sử dụng cuộn cảm cho các máy thu vô tuyến. LNA không có cuộn cảm bao gồm một bộ khuếch đại cấu trúc nguồn chung sử dụng lại dòng kết hợp với một mạch phản hồi tích cực dòng thấp để đạt được phối hợp trở kháng đầu vào dải rộng và tạp âm thấp. Trong LNA, chúng tôi đề xuất sử dụng kỹ thuật điện trở suy giảm để cải thiện độ tuyến tính của mạch. Thêm vào đó, chúng tôi thiết kế chế độ đi vòng cho mạch LNA để mở rộng phạm vi ứng dụng của mạch. LNA đề xuất được thực hiện trên công nghệ CMOS 28 nm. LNA có hệ số khuếch đại 14.9 dB và băng thông 2.2 GHz. Hệ số tạp âm (NF) là 1.95 dB và điểm chặn đầu vào bậc 3 (IIP3) là 24.8 dBm tại 2.3 GHz. Mạch tiêu thụ 17.2 mW với nguồn cung cấp 0.9 V và có diện tích chiếm trên chip là 0.011 mm^2.

Từ khóa: Không sử dụng cuộn cảm; Sử dụng lại dòng; Phản hồi tích cực; Dải rộng; Độ tuyến tính cao; Khuếch đại tạp âm thấp.