

Design and simulation of a 15-bit successive approximation register analog-to-digital converter

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ABSTRACT

Analog-to-digital converters (ADC) are widely employed to monitor long-term signal characteristics in wireless sensor networks and healthcare electronic devices. It is critical in these applications to use an energy-efficient ADC to extend battery life. This paper presents a 15-bit successive approximation register (SAR) ADC for using in biomedical processing systems. The segmentation degrees (the amount of bits in each divided capacitive sub-array) are optimized to minimize switching power and area based on linearity and matching requirements. The proposed SAR ADC is simulated by using Matlab Simulink. The simulated results show that the ADC achieves 14.78-bit of effective numbers of bits (ENoB), 111.5 dB of the spurious-free dynamic range (SFDR) with 90.74 dB of signal-to-noise ratio (SNR) at a sampling rate of 10 MHz.

Keywords: Analog-to-digital converters; Successive approximation register; Binary weighted with attenuation capacitor.

1. INTRODUCTION

Low power consumption is necessary for portable biomedical sensing applications to run for extended periods on batteries. The low-frequency bandwidth of human biopotentials is up to a few kHz. An electrocardiogram (ECG) has an amplitude of around 1 mV [1]. An electroencephalogram (EEG) has a frequency range of 0.5 Hz to 150 Hz and an amplitude range of 10 to 100 μ V [2]. The normal amplitude of the local field potential (LFP), which ranges from 1 Hz to 200 Hz, is 1 mV [3]. Since the biopotentials are low-amplitude signals, signal processing must first be done on them. The analog-to-digital converter (ADC) will be the following significant building component for signal processing. The accuracy of the observed biopotentials is thus dependent on the performance of the amplifier and ADC. The successive approximation register (SAR) ADC is commonly utilized in low-power applications [4]. The performance of capacitive-array DAC, as one of the main building blocks of SAR ADC, affects the linearity, conversion speed, power consumption, and area of SAR ADC. Among the various DACs used in SAR ADC, the binary-weighted capacitive-array with attenuation capacitor (BWA) DAC has gotten a lot of attention [5-7]. The BWA structure is a variant of the traditional binary-weighted capacitor-array (CBW) [8] in which one or more attenuation capacitors $C_{AT1,2}$ are used to divide the CBW structure into two or more sub-arrays. The unit capacitor in the BWA structure is substantially smaller than in the CBW structure. The BWA structure has been improved in several approaches [5-7]. The fractional BWA (FBWA) DAC [5] reduces input capacitance by using a fractional attenuation capacitor, although these results lead to poor matching with other capacitors. For this construction to achieve linearity requirements, calibration is frequently required. The mismatch problem is addressed by non-fractional BWA (NFBWA) DAC [6]. Another NFBWA design [7] makes use of integer multiples of the unit capacitor as the

attenuation capacitor to achieve strong matching at the expense of area efficiency. However, in order to meet the radix-2 ratio, the dummy capacitor $C_{AT1,2}$ is removed, resulting in a Least Significant Bit (LSB) is lost [2].

In this paper, an NFBWA DAC is presented to minimize power consumption and space while also addressing issues with traditional BWA DACs. Matlab Simulink is used to simulate the behavior of a 15-bit SAR ADC with proposed DACs then compared with the ideal DAC. The segmentation degree and related unit capacitor values in both sub-arrays are determined based on performance and matching requirements. When compared to standard CBW and BWA procedures, the results demonstrate an improvement in both energy and area.

2. THE PROPOSED ARCHITECTURE

The successive approximation register (SAR) ADC is the best option among the various converter architectures because of its low power consumption, excellent conversion accuracy and with an easy-to-understand design [8-9]. The binary search technique is used in the SAR ADC, which requires a simple structure consisting of a sample and hold (S/H), comparator, digital-to-analog converter and block of successive approximation register [10]. This topology is commonly utilized to create medium-high resolution ADCs for medium-low speed applications. In this paper synchronous SAR logic is chosen as the control block to evaluate the proposed designs. The SAR controller compares V_{IN} and V_{DAC} and digitally modifies the power supply to the DAC in accordance with the comparison results, as illustrated in Figure 1. The SAR logic creates sampling control signals for the S&H switch and control signals for the DAC switch drivers in the differential capacitive DAC using the hybrid switching approach. The benefit of this binary search approach is that it is quicker than the direct search method because one cycle is needed for each resolution bit. In other words, the iterative search method's necessary number of comparisons is a linear function of resolution instead of an exponential one, which results in greater energy efficiency.

DACs are important in determining the SAR ADC line, in addition to noise and speed, among other factors. Indeed, the differences between capacitors used in DAC are an important source of linear failure [11]. Additionally, the switching method has an effect on the amount of power used by the converter. Figure 2 shows the block diagram of the 15-bit in Matlab Simulink.

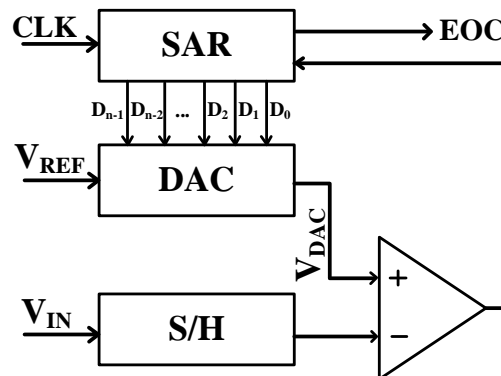


Figure 1. The typical structure of SAR ADC.

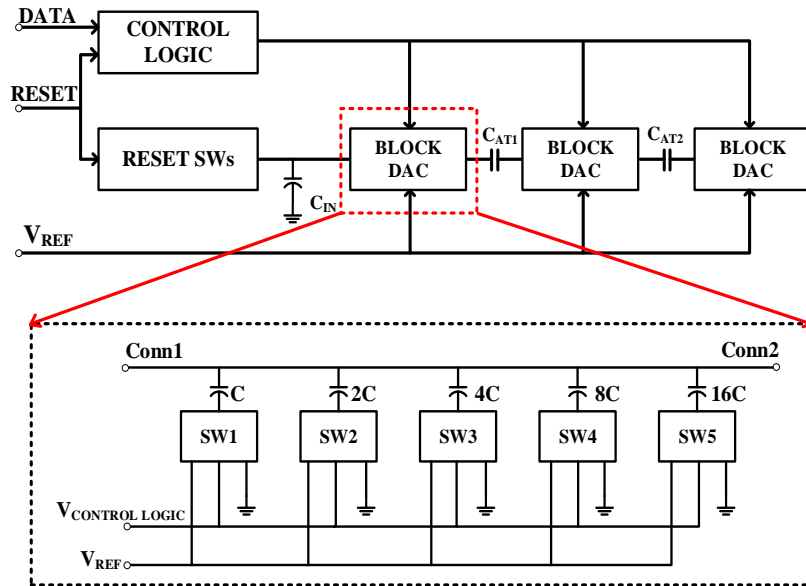


Figure 2. The block diagram of the 15-bit DAC in SIMULINK.

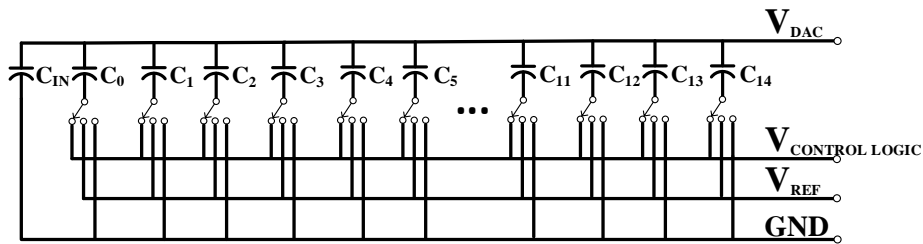


Figure 3. The conventional design of CBW DAC.

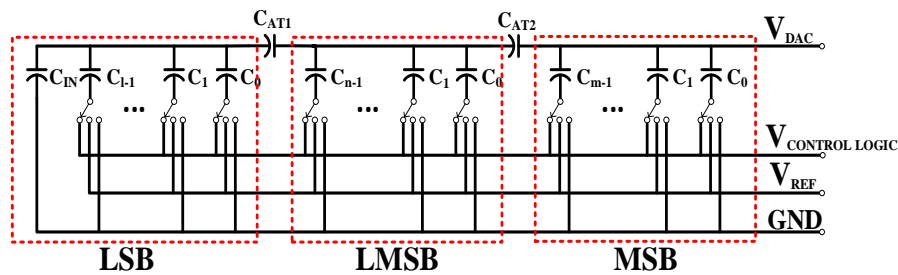


Figure 4. The proposed of 15 bit NFBWA DACs.

Figure 3 depicts a single-ended N-bit multi-segmentation NFBWA DAC architecture with attenuation capacitors which are multiples of the unit capacitor to improve mismatch tolerance. The DAC array is divided into three sub-arrays with $m : n : 1$ bit width ratio. The most significant bit (MSB) subarray has m bits and corresponds capacitors $C_0 \sim C_{m-1}$. The few-MSB (FMSB) subarray consists of n bits and capacitors $C_0 \sim C_{n-1}$. To achieve the maximum linearity in the DAC, the LSB subarray employs l -bit LSB segmentation (with $m = n = l = 5$ and $C_{IN} = C$ with $C = 0.1$ to 1pF). The design strategy of the proposed architecture is explained as follows. As shown in Figure 4, the left and right parts of C_{AT1} are LSB and LMSB subarrays while the left and right parts of C_{AT2} are LMSB and MSB subarrays, respectively. Within each subarray, all the capacitors are assigned according to

the radix-2 ratio. This architecture uses fewer unit capacitors than a typical binary-weighted (CBW) capacitive-array DAC shown in Figure 3, which considerably decreases the charging time-constant and switching energy. With other capacitors, NFBWA employs a fractional multiple of the unit capacitors, which is not precise in the layout due to the limited lithography production grid and a poorer matching with other capacitors. Moreover, the parasitic effects of the BWA DAC drastically reduce the ADC's integral and differential nonlinearity yields. So the value of capacitor in the proposed DAC is set to the equivalent capacitance approximation C or $C \sim C_{AT} = (\text{sum unit capacitor of LSB array}) / (\text{sum unit capacitor of MSB array})$ for the attenuation capacitor C_{AT} . This ensures that the series connection of LSB subarray and $C_{AT1,2}$ matches C_{IN} . In this way, the bit-related capacitors $C_1 \sim C_{n,m,l}$ can generate voltages in radix-2 form while avoiding the use of fractional attenuation capacitors. In the case of the pure C-2C structure, the entire structure may be divided into N subarrays. Because there is only 5 MSB-bit, the gain mistake has no influence on the ADC's linearity and the impact of gain errors in less-significant bit subarrays would deteriorate linearity performance. As a result, using the C-2C configuration with one MSB bit of other NFBWA for high resolution DAC with rigorous linearity requirements is impracticable. The linearity performance of a capacitive DAC with the BWA structure is mostly influenced by parasitic and mismatch concerns. Gain error is caused by parasitic capacitance on the top plate of each subarray. The parasitic capacitances of the LSB, LMSB, and MSB subarrays in the proposed structure are denoted as C_{IN} , C_{m-1} , and C_{n-1} , respectively, in figure 4. The gain error induced that the C_{IN} has no effect on the linearity performance of the MSB subarray [12]. The gain errors of the LMSB and LSB subarrays are examined in the next section by using the gain of the MSB subarray as a reference without taking the capacitor mismatch into account.

3. RESULTS AND DISCUSSION

To achieve the linearity criteria, the predicted dynamic performance signal-to-noise and distortion ratio (SNDR) for a 15-bit SAR ADC should be more than $6.02(N-1)+1.76$ dB, which means $(N-1)$ effective number of bits (EN_{OB}). As a result, the SNDR of the proposed 15-bit DAC should be more than 85.95-dB. In Matlab, a 15-bit SAR ADC behavioral model with the proposed NFBWA DAC is simulated to determine the matching need for each segmentation degree. Except for the DAC block, the construction blocks such as comparator, S/H switch, and digital control switches are believed to be perfect, therefore the dynamic performance of the DAC will ultimately define the performance of the SAR ADC.

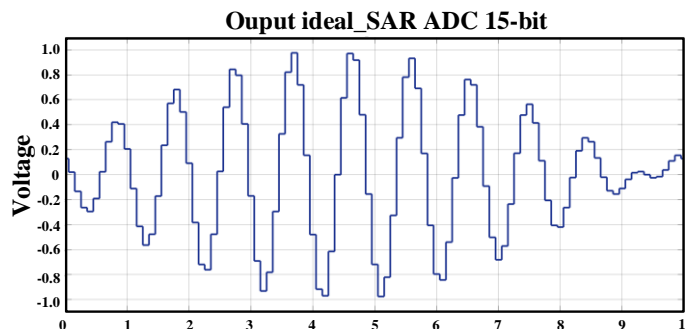


Figure 5. The signal of ideal DAC block.

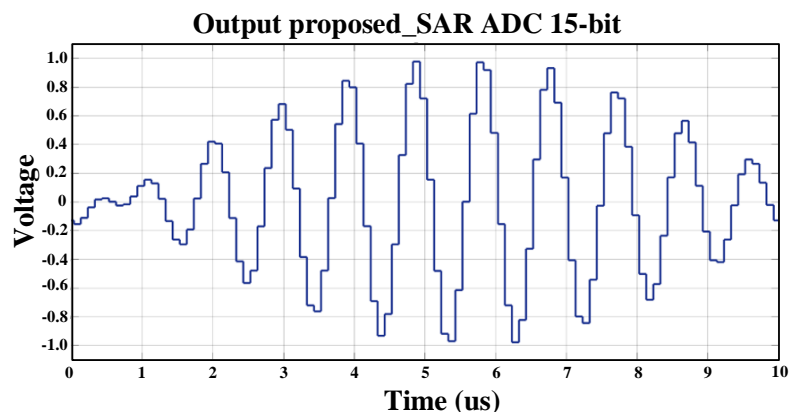


Figure 6. The signal of proposed DAC block.

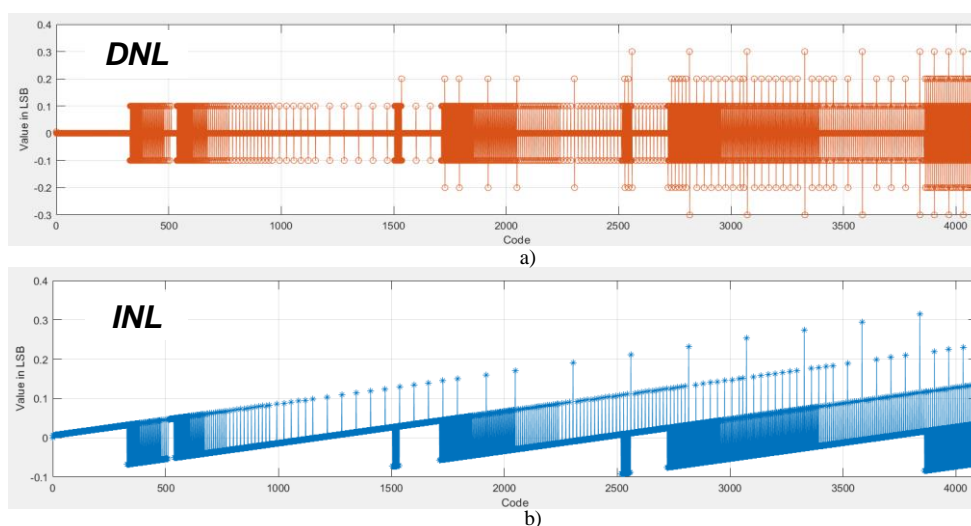


Figure 7. Simulated results of the DNL and INL.

For high-resolution DACs, the split array minimizes the total capacitor area required. The main part of the frequency detection unit of the proposed configuration unit, which determines the frequency of the analog input signal based on the operating clock frequency and the sampling rate of the selected ADC, is the proposed 15-bit SAR ADC. The proposed ADC was simulated for the intended specifications in order to verify the proposed behavioral model of the ADC and comprehend the consequences of various non-ideal elements. With f_{sample} of 10 MHz and the input signals at $2V_{P-P}$, to validate the proposed behavioral model of the ADC and understand the consequences of various non-idealities, the proposed ADC was simulated for the desired specifications. The output waveforms of the reconstructed signals by the proposed ideal and non-ideal 15-bit configurable SAR ADC are shown in Figure 5 and Figure 6. For the proposed analysis, a transistor-level simulation was performed for a 15-bit NFBWA converter with simple gating. The simulation results are shown in Figure 7. As expected, the DNL has periodic pattern featuring a codes of range about $-0.3/0.3$ while INL is the range $-0.1/0.6$ LSBs. Additionally, we achieve an SNR of up to 90.74 dB, which is equivalent to a 15-bit effective bit count (ENoB). Furthermore, the non-ideal DAC's total harmonic distortion

(THD) is -13.67 dB. The ideal situation of 111.50 dB and 90.74 dB results in the spurious-free dynamic range (SFDR) and signal to noise ratio (SNR).

Because the influence of capacitor mismatch from the MSB sub-array dominates dynamic performance [13], simulations are performed to estimate the maximum mismatch standard deviation for MSB based on the SNDR requirement. From Table 1, it can be seen that the area of this proposal is significantly smaller than that of the other structures. Moreover, the ENoB parameter is also more efficient than the other structures. Table 2 shows a comparison with some other topologies. Although the 9.18-bit high performance is achieved using the CBW structure in [6,] the INL and DNL are excessively big, resulting in extremely huge errors in the circuit and almost inaccurate ADC operation. Moreover, ENoB with a similar structure to 12-NFBWA [16] achieved only 10.47 bits at sampling rate of 1K/s while it achieved 14.78-bit with the proposed 15-bit SAR ADC at sampling rate of $f_{sample} = 10$ MS/s. It means that the accuracy of ADC increases significantly.

Table 1. Performance comparison of 15-bit capacitive DACs with various structures.

Design	MSB:FMSB:LSB	Area (C)	Calibration Block	Unit Cap. Ratio	Energy (C.Vref ²)	ENoB
CBW	8:7:0	32768	No	1	4368	15.01
NFBWA [7]	8:0:4	2072	No	2	182.0	11.64
NFBWA [15]	10:1:1	32768	No	4	4368	10.47
This work	5:5:5	482(1/5)	No	3	12.84	14.78

Table 2. Performance summary and comparison of the ultra-low-speed SAR ADCs.

Design	[6]	[14]	[15]	[16]	This work
Topology	CBW	BWA	BWA	NFBWA	NFBWA (BWA)
Bit	10	5	5	12	15
Sampling rate (MS/s)	50	500	800	1K	10
Clock Mode	Syn.	Asyn.	Asyn.	Syn.	Syn.
DNL (LSB)	+0.91/-0.63	0.26	-0.56/+0.53	+0.35/-0.41	-0.3/+0.3
INL (LSB)	+1.27/-1.36	0.16	-0.62/+0.61	+0.6/-0.74	-0.1/+0.6
ENoB	9.18	4.10 (with $f_{in}=120$ MHz)	4.52/4.40	10.47	14.78

4. CONCLUSIONS

In this paper, an energy efficient and space saving NFBWA DAC design is presented and simulated in Matlab Simulink. In this work, a 15-bit 10MS/s SAR ADC for biomedical signal processing is presented. By combining the proposed 3-segmentation

NFBWA DAC, a comprehensive design approach for a 15-bit SAR ADC with the proposed DAC is provided to minimize the power consumption and capacitive array size. The proposed approach outperforms other traditional BWA algorithms in terms of ENOB and SNR while maintaining good matching at sampling rate of 10 MS/s.

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TÓM TẮT

Thiết kế và mô phỏng bộ chuyển đổi tương tự sang số 15-bit sử dụng thanh ghi xấp xỉ kế tiếp trên Matlab

Bộ chuyển đổi tương tự sang số (ADC) được sử dụng rộng rãi để giám sát các đặc tính tín hiệu dài hạn trong các mạng cảm biến không dây và các thiết bị điện tử chăm sóc sức khỏe. Điều quan trọng trong các ứng dụng này là sử dụng bộ ADC tiết kiệm năng lượng để kéo dài tuổi thọ pin. Trong bài báo này, một đề xuất bộ ADC thanh ghi xấp xỉ liên tiếp (SAR) 15 bit cho các hệ thống xử lý y sinh được trình bày. Các mức phân đoạn (số bit trong mỗi mảng con điện dung được chia nhỏ) được tối ưu hóa để giảm thiểu công suất và diện tích chuyển đổi dựa trên các yêu cầu về tuyến tính. SAR ADC đề xuất được mô phỏng bằng Matlab Simulink. Kết quả mô phỏng cho thấy bộ ADC đề xuất đạt được số bit hiệu dụng (ENoB) là 14,78 bit, dải động không giả (SFDR) là 111,5 dB và tỷ lệ tín hiệu trên tạp âm (SNR) là 90,74 dB ở tốc độ lấy mẫu 10 MHz.

Từ khoá: Bộ chuyển đổi tương tự - số; Thanh ghi xấp xỉ kế tiếp; Trọng số nhị phân với giảm tụ điện.